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Non-Quasi-Static Modeling of Printed OTFTs

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ABSTRACT A non-quasi-static compact model well suited for the simulation of the electrical behavior of printed organic thin-film transistors (OTFTs) is proposed and validated. The model is based on the discretization of the current continuity equation by using a spline collocation approach while the electrical transport in the organic semiconductor is described by the variable range hopping theory. The model accounts for the presence of parasitic regions that are often found in the layouts of printed OTFTs due to large process tolerances. The model has been implemented in the Verilog-A language and has been validated by a comparison with the capacitance vs. voltage (small signal) characteristics of the devices and measurements made on OTFT-based common-source amplifiers (large signal). A comparison with a quasi-static version of the model is reported.

INDEX TERMS SPICE modeling, non-quasi-static modeling, organic thin-film-transistors, printed organic electronics, large signal model.

I. INTRODUCTION

Printed organic electronics has received great attention in recent times since it is a promising technology for the mass production of several applications on large area and on flexible substrates. Moreover, the possibility to use only low-temperature processes is a key feature for achieving very low production costs.

In order to successfully design organic electronics applications there is a need for compact models that can be profitably used in Electronic Design Automation software environments. Several compact models have been proposed: most of them are charge-based models that are able to reproduce the static and the quasi-static (QS) operation of Organic Thin Film Transistors (OTFTs) [1], [2], [3]. But, due to the relatively low carrier mobility and the large geometrical sizes associated with printing processes, the cut-off frequencies of the devices are often found in the tens of kilohertz range [4]. Hence, OTFTs are likely to operate in the non-quasi-static (NQS) regime. Despite the fact that the necessity of NQS models has been claimed several years ago [5] and it is recognized as one of the challenges of OTFT compact modelling [6], it is only recently that some effort has been devoted to the realization of models accounting for non-quasi-static effects for these devices [4], [7], [8].

Several compact models addressing NQS effects in high-frequency operation have been developed for crystalline silicon MOSFETs [9], [10], [11]. Nevertheless, it is not possible to directly use these models for printed OTFTs since the physics underlying the operation of the organic-based MOSFETs relies on different assumptions such as electrical transport ruled by variable range hopping, carrier mobility that is a function of carrier density, presence of trap states with large time constants, and so on.

Moreover, practical layout of printed OTFTs often shows relatively large parasitic regions that extend well beyond both sides of the channel, in which the organic semiconductor (OSC) layer is still surmounted by the gate electrode and contributes to the overall device capacitance. These parasitic regions are found quite commonly in literature when high throughput roll-to-roll techniques are used (as

an example, see the micrographs reported in [4], [12], [13], [14]). Being related to the geometric tolerances between consecutive printing steps, these areas are often much larger than the channel length itself.

In this work, we report a non-quasi-static model that: i) implements variable range hopping (VRH) theory as charge-transport mechanisms; ii) is based on the current continuity equation and accounts for NQS operation; iii) accounts for the presence of parasitic regions. The model has been implemented in Verilog-A and has been validated by comparing the simulated results with measurements made on OTFTs in static, large- and small-signal regimes.

II. EXPERIMENTAL

A. DEVICE FABRICATION

Fully-printed, multi-fingered Organic Thin Film Transistors, with staggered top-gate configuration, have been fabricated on flexible (100 μm thick) polyethylene-naphtalate (PEN) foil.

The top-gate configuration was chosen because of the needs of the sensing application for which the devices were designed.

Source (S) and drain (D) contacts have been made by ink-jet printer (DIMATIX 2830) and Ag nanoparticle ink (ANP Silverjet DGP 40LT-15C). After deposition, the contacts have been annealed at 100 °C in oven. After SAM treatment of the contacts (to improve carrier injection), the OSC layer (50 nm thick Merck lisicon®SP400, formulated for gravure printing) and the dielectric layer (Cytop CTL-809M) have been sequentially deposited by using the gravure printer "Labratester" by Norbert Schläfli Maschinen AG. Suitable glass clichés have been fabricated using a custom procedure [15]. A multi-step process has been employed for Cytop deposition in order to obtain a gate dielectric layer thickness of 400 nm, that can ensure low gate leakage current. Finally, Ag gate electrodes have been defined by ink-jet printer. Gate contact thickness about 200 nm, S/D about 100 nm thick. The annealing steps for each material are kept under 100°C. The printing technique was chosen according to the features required [16]. Device channel length and width ranged from 30 to 400 μm and from 100 to 900 μm, respectively.

Typical device layout (in scale) is shown in Fig. 1. Since an alternating sequence of inkjet and gravure deposition steps has been used, the geometric tolerances in the device layout have been chosen prudently large: as can be seen from Fig. 1 the distance between the "bus bars", the size of the OSC region and the length of the metal gate have been oversized in order to minimize the possibility of failures due to misalignments in consecutive printing steps. While the channel lengths and widths are still precisely defined, the OTFTs show two very large parasitic regions, that extend on both sides of the source and drain "comb", in which the OSC is surmounted by the gate electrode and contributes to the overall device capacitance. Similar layouts with large parasitic regions are quite common for printed OTFTs and have been already reported in the literature [4], [12], [13], [14].

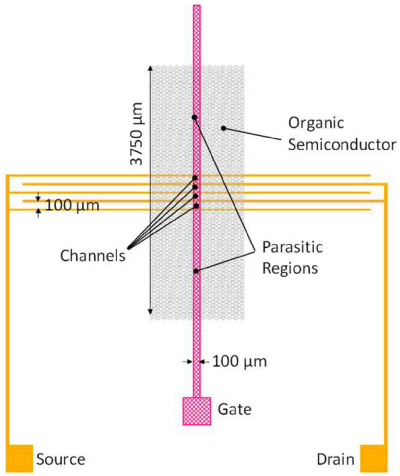

FIGURE 1. Typical device layout (in scale) of the printed OTFTs used in this work.

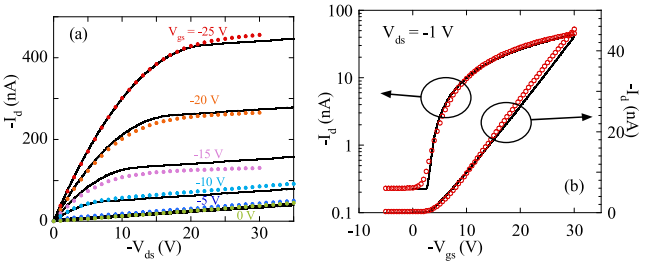

FIGURE 2. DC (static) characterization. (a) Measured (symbols) and simulated (black curves) output characteristics of an L = 100 μm W = 400 μm device measured after light exposure; black lines: simulated output characteristics. (b) Transfer characteristics of the same device measured after light exposure (red symbols); simulated transfer characteristics (black curves). In both panels, the simulated curves have been computed by using eqs. (9), (10), and (11).

B. STATIC (DC) CHARACTERIZATION

DC characteristics have been measured with an HP4145B "semiconductor parameter analyzer". The mobility at low V_{ds}, as deduced from transconductance (g_m) measurements, $\mu = g_m \frac{L}{C_i V_{ds} W}$, is up to $\mu_{LIN} \sim 0.24$ cm^{2}V^{-1}s^{-1} and good linearity has been observed in the ON-region, even for short channel lengths, suggesting small parasitic contact resistance. The devices show low threshold voltage, around –4 V. Gate leakage current is very low, $I_g < 2$ pA at $V_{gs} = -20$ V, thanks to the high quality of the printed dielectric layer. The subthreshold slope is around 4500 mV/dec. These figures compare favorably with state-of-the-art performances that are achieved nowadays on fully-printed OTFTs [13], [17].

Typical output and transfer characteristics are shown in Fig. 2a and in Fig. 2b, respectively: the devices have an on/off ratio of around 2.5 decades and operate in off regime for $V_{gs} = 0$ V. It must be noted that the ratio just reported is affected by a light-induced instability, that disappears after

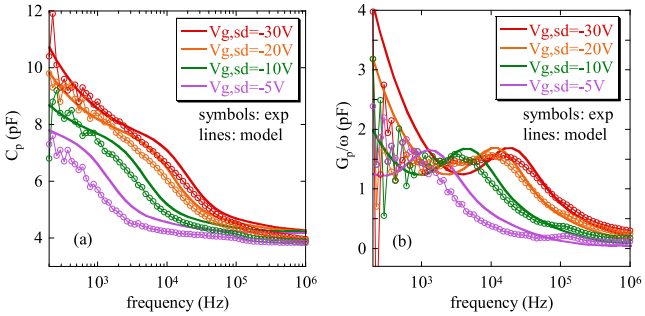

FIGURE 3. (a) Capacitance, C_p, and (b) loss, G_p/ω, as a function of frequency measured (symbols) and simulated (solid lines) on an L = 100 μm W = 400 μm device.

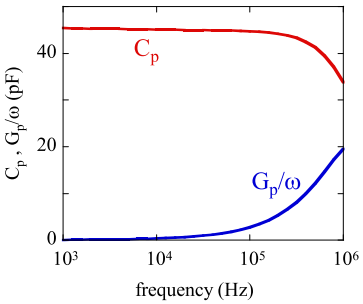

FIGURE 4. Capacitance, C_p, and loss, G_p/ω, as a function of frequency measured on a MIM structure with insulator thickness 400 nm and area 1 mm^2.

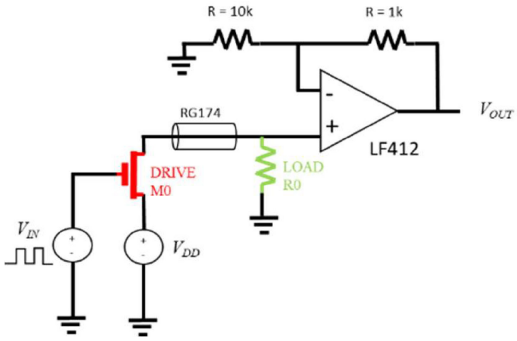

FIGURE 5. Schematic of the circuit used for dynamic characterization of the OTFTs.

few hours of recovery in dark conditions, whose only effect is to increase the magnitude of the off current, slightly reducing the on/off ratio. Since the behavior of the circuits considered in this work is only marginally affected by the details of the off regime, we operated without any particular attention to keep the devices in dark or in a relaxed state.

C. SMALL SIGNAL (C-V) CHARACTERIZATION

Impedance vs. voltage characteristics of the devices have been measured with an HP4192A LCR meter for frequencies ranging from 200 Hz to 1 MHz. In Fig. 3, typical impedance curves as a function of the small signal frequency, measured with source and drain linked and grounded, are reported for different gate-to-source-and-drain ($V_{g,sd}$) bias for an L = 100 μm, W = 400 μm device. The amplitude of the modulation signal was δV_g = 1V.

The measured impedances are reported as the capacitances (C_p) and conductances, normalized to the angular frequency (G_p/ω) of an equivalent parallel RC circuit. The C_p vs f curves clearly show a decreasing trend as f is increased: focusing on the $V_{g,sd}$ = 30 V curves, the measured C_p monotonically decreases from 10 pF at low frequency to reach an asymptotic high-frequency value of 4 pF, after a noticeable inflection around $f \sim 10$ kHz. If we consider only the channel regions of the device and the gate-to-source and gate-to-drain overlap capacitances we would obtain $C_p \approx$ 6 pF. Instead, the measured C_p at low frequency is much higher than this value: this very high value is related to the presence of the parasitic regions, as will be confirmed by simulations in the following sections.

The G_p/ω trend, aside from the huge noise at low frequencies, shows a relatively broad peak for $f \sim 15$ kHz at $V_{g,sd}$ = 30 V, just after the inflection occurring in the C_p curve: this suggests that the intrinsic cut-off frequency (f_T) of the device is around 10 kHz. Indeed, if we compute the unity gain frequency f_1 with the usual textbook formula [18], $f_1 = g_m/(2\pi C)$ with g_m being the transconductance in saturation regime, we obtain an estimate of $f_1 \approx 7.7$ kHz. As the gate bias is reduced, the G_p/ω peak moves to lower frequencies, as expected from MOSFET theory [19].

The trend of the CV characteristics is not related to a non-ideal behavior of the gate insulator material (Cytop CTL-809M, see Section II-A). Actually, capacitance measurements made on metal-insulator-metal (MIM) structures, fabricated with the same processing steps of the OTFTs, show that the frequency dependence of the dielectric constant of the gate insulator is negligible in the frequency range taken into consideration and, in this range, the behavior of the insulator can be assumed as ideal. In fact, the C_p vs f measurements reported in Fig. 4, taken with a small signal amplitude of 1 V superimposed to a constant bias V_{bias} = 0 V, show no appreciable variations for frequencies f < 500 kHz with a negligible value of G_p/ω. For f > 500 kHz there is a small decrease of C_p and a rise of G_p/ω indicating that the cut-off frequency of the MIM structure is in this range.

D. LARGE SIGNAL (DYNAMIC) CHARACTERIZATION

In order to validate the large signal model, we measured the dynamic response of an OTFT-based common-source (CS) amplifier, operated with a large voltage pulse as input signal. The schematic of the circuit is shown in Fig. 5. The device under test (M0) is contacted in a probe station and the DC voltage generator V_{dd} is connected to the source in order to work with positive voltage. The pulse generator, V_{IN}, is connected to the gate to provide the input signal. The load resistance (R0, 30 MΩ) is located on a separate circuit board and is connected to the drain of M0 through

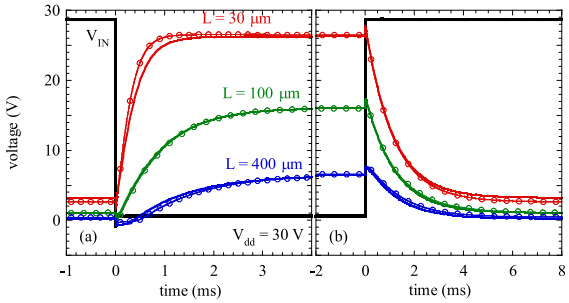

FIGURE 6. (a) Turn-on and (b) turn-off transients of the CS amplifier schematized in Fig. 5 using devices with different channel lengths. The voltage supply V_{dd} (30 V) and the input signal V_{IN} (black lines) are the same in each case. Symbols + thin lines: measurements; thick lines: simulations.

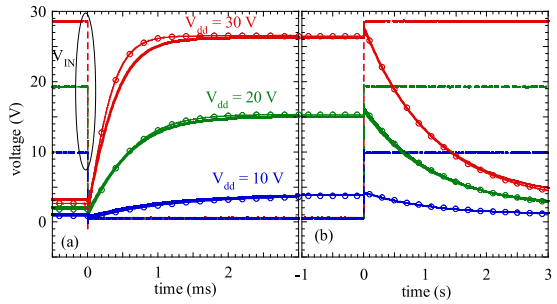

FIGURE 7. (a) Turn-on and (b) turn-off transients of the CS amplifier schematized in Fig. 5, using an L = 30 μm W = 400 μm device, operated with different voltage supplies (V_{dd}) and input signal swings (V_{IN}). Symbols + thin lines: measurements; thick lines: simulations.

a coaxial cable, (RG174, ≈30 cm long). The CS amplifier has a very high output resistance, of the same order of magnitude of R0, making not viable a direct connection to the input of an oscilloscope that has a much lower input resistance (typically 1 to 10 MΩ). Hence, on the separate circuit board, a non-inverting feedback amplifier, based on the LF412 integrated op-amp, has been implemented, acting as a buffer stage between the output of the CS amplifier and the measuring instrumentation. In fact, the LF412 has an input resistance of the order of 10^{12} Ω [20], that is high enough to be seen as a small perturbation in the operation of the circuit under test.

In order to minimize the effects of the electrical interferences, we have used input signal frequencies that are not multiple of the power line frequency (50 Hz) and the output signals collected have been averaged over 128 consecutive acquisitions. Moreover, the connection between the CS amplifier and the buffer stage has been made by using a RG-174 coaxial cable: while this approach is effective in order to shield electromagnetic interferences, it introduces in the circuit a transmission line that is not matched at both ends (the characteristic impedance of RG-174 is 50 Ω) and introduces an additional delay time.

Typical turn-on and turn-off transients measured on the CS amplifier using devices with different channel lengths are shown in Fig. 6. In Fig. 7 are reported the transients of the CS amplifier using an L = 30 μm W = 400 μm device, when it is operated with different voltage supplies (V_{dd}) and input signal swings (V_{IN}).

III. MODEL

A. DC MODEL

The microscopic physical model describing the organic semiconductor used in this work has been originally proposed in [21] and is based on the variable range hopping (VRH) theory [22]. The basic assumption is that the mechanism responsible for the electrical current is the thermal-activated tunneling of charge carriers between localized states with energy near the Fermi level. These states are randomly distributed in space and energy and their energy distribution function is an exponential tail with characteristic energy E_0, that in the following we express also in voltage (V_{T_0}) and temperature (T_0) units

$$E_0 = qV_{T_0} = kT_0 \tag{1}$$

where q is the elementary charge and k is the Boltzmann constant. When the VRH theory is applied to a "MOS-like" structure, it is found that the field effect induced charge for unit surface, Q, for an n-type semiconductor, is given by [21]:

$$Q = -Q_0 \exp\left(\frac{\varphi - V}{2V_{T_0}}\right) \tag{2}$$

where $Q_0 = \sqrt{2kT_0N_t\varepsilon_s}$, φ is the electrostatic potential at the semiconductor–insulator interface (i.e., the surface potential), V is the channel potential, N_t is the number of occupied states per unit volume in the bulk, and ε_s is the semiconductor dielectric permittivity. The channel conductance, $G(y)$, is defined by the following relation that links the current $I(y)$ that flows in the channel of the OTFT at a point of coordinate y and the gradient of the channel potential $\partial V/\partial y$ at that point:

$$I(y) = WG(Q(y))\frac{\partial V}{\partial y} \tag{3}$$

where W is the channel width.

In the framework of the VRH theory, the channel conductance is given by [21]

$$G(Q) = G_0\left(-\frac{Q}{Q_0}\right)^{\gamma-1} \tag{4}$$

with $\gamma = 2T_0/T$, where G_0 is the bulk organic semiconductor conductance and T is the device temperature.

An expression for Q is also obtained by applying the Gauss theorem to the metal-insulator-organic semiconductor structure and is given, as usual, by:

$$Q = -C_i(V_g - V_{fb} - \varphi) \tag{5}$$

where C_i is the insulator capacitance for unit area, V_g is the gate bias, and V_{fb} is a reference voltage that plays the role of the flat band voltage in the standard MOS theory.

By equating the expressions for Q given by (2) and (5) we obtain an equation for the surface potential as a function of the channel potential $\varphi = \varphi(V)$. The expression for φ is particularly simple if we make use of the Lambert W function, here indicated as lw(x):

$$\varphi(V) = V_g - V_{fb} - 2V_{T_0}\,\mathrm{lw}\left(\frac{Q_0}{2V_{T_0}C_i}\exp\left(\frac{V_g - V_{fb} - V}{2V_{T_0}}\right)\right) \tag{6}$$

and, substituting the solution in (2), we can express also Q as a function of V, $Q = Q(V)$. In particular, it is possible to determine the induced charge at source and drain end of the channel, $Q_s = Q(V_s)$ and $Q_d = Q(V_d)$.

From (2) and (5) a differential relation between the dQ and dV can be derived:

$$dV = \left(\frac{1}{C_i} - \frac{2V_{T_0}}{Q}\right)dQ. \tag{7}$$

Making use of this relation, the channel current (3) can be expressed as a function of Q:

$$I(y) = WG(Q(y))\left(\frac{1}{C_i} - \frac{2V_{T_0}}{Q(y)}\right)\frac{dQ}{dy}. \tag{8}$$

Hence, the VRH theory provides a very simple expression for the channel current, in which the channel conductance depends only by $Q(y)$ with a power law (4) and the "driving force" for the current is proportional to dQ / dy (8). Therefore, the integration of (8) along the whole channel length, L, is straightforward and gives the expression for the channel current in static (DC) conditions:

$$I_{DC0} = G_0\frac{W}{L}\left[\frac{Q_0}{C_i}\left(\frac{u_s^{\gamma} - u_d^{\gamma}}{\gamma}\right) + 2V_{T_0}\left(\frac{u_s^{\gamma-1} - u_d^{\gamma-1}}{\gamma - 1}\right)\right]. \tag{9}$$

with u_s and u_d the normalized charges at source and drain end of the channel, $u_s = -Q_s$ / Q_0 and $u_d = -Q_d$ / Q_0.

The off current is taken into account by introducing a backchannel resistivity per unit square, ρ_{off}, not modulated by the gate bias, that is equivalent to a parallel series resistance between source and drain terminals. Hence the overall current is given by

$$I_{DC} = I_{DC0} + I_{off} \tag{10}$$

with

$$I_{\mathrm{off}} = \frac{V_{ds}}{\frac{L}{W}\rho_{off}} \tag{11}$$

The simplicity of the expressions obtained in the framework of the VRH theory and its small number of free parameters are the main reasons why this approach has been chosen in order to develop the LS-NQS model that will be presented in the following sections. However, despite its simplicity, the VRH theory provides an acceptable reproduction of the transfer and output characteristics shown in Fig. 2a and in Fig. 2b, respectively. Nevertheless, in principle, it is possible to use more refined models at the expense of an additional analytical complexity of the equations governing the time dependence of the charge density and the channel current.

B. NON-QUASI-STATIC (NQS) MODEL

Due to their relatively low field effect mobility, printed OTFTs enter an NQS regime when they are operated at frequencies of the order of a few kilohertz (see Section II-C). In this regime, the carriers are unable to follow the rapid variation of the electrical potential inside the device and their instantaneous distribution differs from the distribution obtained in the DC case. Hence, in NQS regime, I and Q appearing in (8) become also functions of time: $I = I(y, t)$, $Q = Q(y, t)$.

The instantaneous carrier distribution, $Q(y, t)$, can be obtained by solving the current continuity equation, that, with the sign convention used in the previous sections, reads:

$$\frac{\partial I}{\partial y} = W\frac{\partial Q}{\partial t} \tag{12}$$

Substituting (8) and (4) in (12), expanding the space derivative and making use of the dimensionless quantity $u(y, t) = -Q(y, t)/Q_0$, the following equation is obtained:

$$\frac{\partial u}{\partial t} = G_0\left[\left(\frac{\gamma - 1}{C_i}u^{\gamma-2} + \frac{\gamma - 2}{Q_0/(2V_{T_0})}u^{\gamma-3}\right)\left(\frac{\partial u}{\partial y}\right)^2 + \left(\frac{1}{C_i}u^{\gamma-1} + \frac{1}{Q_0/(2V_{T_0})}u^{\gamma-2}\right)\left(\frac{\partial^2 u}{\partial y^2}\right)\right] \tag{13}$$

The non-linear partial derivative equation (PDE) (13) governs the time evolution of the carrier distribution in the OTFTs channel regions as well as in the parasitic regions outside the channel. The difference in the two cases resides in the boundary conditions that have to be imposed at the two ends of the regions in which (13) is solved:

- In channel regions, it is assumed that the source and drain contacts are in equilibrium with the organic semiconductor, i.e., the contacts have an infinitely high recombination velocity and Q_s and Q_d (and the corresponding dimensionless quantities u_s and u_d) can be computed by using (5) and (6). This is the usual boundary condition that is imposed in the presence of ohmic contacts: actually, the metal/organic semiconductor junction is much more similar to a Schottky junction [5], [23], but the approximation of ohmic contacts can be still employed in long channel OTFTs, where the device resistance is dominated by the channel resistance and contact effects can be neglected. This assumption indeed limits the range of applicability of the present theory to long-channel devices, but, if different and more appropriate boundary conditions are provided, the present model could be applied also to short-channel devices.

Once the PDE is solved, it is possible to compute the source, drain and gate currents by evaluating the

Ward-Dutton integrals [16]:

$$I_s = -I_{DC} - WQ_0 \int_0^L \left(1 - \frac{y}{L}\right) \frac{\partial u}{\partial t} dy$$
$$I_d = I_{DC} - WQ_0 \int_0^L \frac{y}{L} \frac{\partial u}{\partial t} dy$$
$$I_g = -(I_s + I_d) \tag{14}$$

- In parasitic regions it is assumed that the metal contact is in equilibrium with the organic semiconductor, while, on the other boundary, we impose that the current flow is zero and the electrostatic and channel potentials are floating. In this case, the current entering from the contact (I_c) is computed as:

$$I_c = WQ_0 \int_0^L \frac{\partial u}{\partial t} dy \tag{15}$$

C. DISCRETIZATION

Following the approach described in [17] and [18], to discretize (13) a spline collocation method is used. The overall interval on which the PDE (13) has to be solved is split into n sub-intervals. The extrema of these sub-intervals are the $n + 1$ collocation points, and in the $i - th$ sub-interval, where y ranges from $(i-1) \times L/n$ to $i \times L/n$, the solution of the PDE (13) is approximated with a cubic spline:

$$u(y,t) \approx a_i + b_i x + c_i x^2 + d_i x^3 \quad \frac{i-1}{n} \le x < \frac{i}{n}$$
$$i = 1 \ldots n \tag{16}$$

in which the dimensionless channel coordinate $x = y/L$ has been introduced and it is understood that the coefficients of the cubic spline (a_i, b_i, c_i, and d_i) are only functions of time. These coefficients are determined by imposing the conditions that the spline must observe in order to avoid discontinuities of $\frac{\partial u}{\partial t}$ across sub intervals (see (13)): (i) the spline must interpolate the $n-1$ internal collocation points (x_i, u_i) with $x_i = (i-1)/n$ and i ranging from 2 to n, (ii) the spline must be continuous, (iii) the first and (iv) second derivatives of the spline must be continuous as well. Hence, by imposing these conditions, it is possible to write a linear system that can be solved to determine the splines coefficients:

$$\begin{aligned}
&i)\ \ a_i + b_i x_i + c_i {x_i}^2 + d_i {x_i}^3 = u_i \\
&ii)\ \ a_{i-1} + b_{i-1} x_i + c_{i-1} {x_i}^2 + d_{i-1} {x_i}^3 = a_i + b_i x_i + c_i {x_i}^2 + d_i {x_i}^3 \\
&iii)\ \ b_{i-1} + 2c_{i-1} x_i + 3d_{i-1} {x_i}^2 = b_i + 2c_i x_i + 3d_i {x_i}^2 \\
&iv)\ \ 2c_{i-1} + 6d_{i-1} x_i = 2c_i + 6d_i x_i \\
&\qquad\qquad i = 2 \ldots n
\end{aligned} \tag{17}$$

Actually, the linear system (17) provides only $4n-4$ equations, four for each internal collocation point, while we have $4n$ unknowns: the remaining 4 equations that are needed are found requiring the nullity of the second derivatives on $x = 0$ and $x = 1$ (natural boundary conditions: this is just a mathematically convenient assumption) and imposing the physical boundary conditions in these two points. In the case of a channel region, assuming that source and drain contacts are located at $x = 0$ and $x = 1$ respectively, the physical boundary conditions are (see the discussion in Section III-B):

$$\begin{aligned}
a_1 &= u_s \\
a_n + b_n + c_n + d_n &= u_d
\end{aligned} \tag{18}$$

where u_s and u_d are determined by using (2) and (6). In the case of a parasitic region, assuming that at $x = 0$ there is a contact c (source or drain), the physical boundary conditions that have to be imposed are:

$$\begin{aligned}
a_1 &= u_c \\
b_n + 2c_n + 3d_n &= 0
\end{aligned} \tag{19}$$

where the second line expresses the vanishing of $\frac{\partial u}{\partial y}$ at $x = 1$ and, hence, a zero current flow on the floating boundary (see (8)). When boundary conditions are included in (17), the solution of this system can be written as a linear combination of the values of the spline at collocation points u_j:

$$a_i = \sum_{j=1}^{n+1} S_{i,j}^{(a)} u_j \tag{20}$$

and similar expressions for b_i, c_i and d_i. In turn, once the coefficients of the splines are known, it is straightforward to evaluate the first and second spatial derivatives of u at the internal collocation points (u_i' and u_i'') as well as the integrals appearing in (14) and (15). Also in these cases, we get linear relationships between these quantities and u_j or their time derivative $\frac{du_j}{dt}$ obtaining:

$$u_i' = \sum_{j=1}^{n+1} M_{i,j}^{(\prime)} u_j \qquad u_i'' = \sum_{j=1}^{n+1} M_{i,j}^{(\prime\prime)} u_j \tag{21}$$

$$\int_0^1 (1-x) \frac{\partial u}{\partial t} dx = \sum_{j=1}^{n+1} M_{i,j}^{(s)} \frac{du_j}{dt} \qquad \int_0^1 x \frac{\partial u}{\partial t} dx = \sum_{j=1}^{n+1} M_{i,j}^{(d)} \frac{du_j}{dt}$$
$$\int_0^1 \frac{\partial u}{\partial t} dx = \sum_{j=1}^{n+1} M_{i,j}^{(c)} \frac{du_j}{dt} \tag{22}$$

It is worth to stress that the various matrices S and M appearing in (20), (21) and (22) depend only on n, the number of sub-intervals used for the discretization. In an implementation of this model, these matrices are precomputed once the parameter n is chosen at the beginning of the calculation and doesn't change during the simulation of the circuit.

Once the expressions (21) for the first and second derivative of u at control points are substituted in (13), the PDE becomes a system of non-linear ordinary differential equations (ODEs) in the unknowns u_j that are functions only of time:

$$\frac{du_i}{dt} = f_i(u_1, u_2, \ldots, u_{n+1}) \tag{23}$$

plus the boundary conditions. In this form, the ODE system (23) can be easily solved in a circuit simulation software environment.

TABLE 1. Parameters used in simulations.

t_{ins}	insulator thickness (measured)	400 nm
ε_{ins}	insulator relative dielectric constant	2.1
ε_{sem}	organic semiconductor relative dielectric constant	3.0
E_0	DOS characteristics energy	27 meV
N_t	DOS prefactor	35.6×10^{15} cm^{-3}
G_0	conductivity prefactor	288×10^3 S/cm
V_{fb}	flat band voltage	-2.64 V
ρ_{off}	off state residual resistance	18×10^9 ohm/□

D. VERILOG-A IMPLEMENTATION

The model just presented here has been implemented in the Verilog-A language. The program has been designed with the aim to be easily adapted to device layouts with parasitic regions that can be different in shape, position and number. Hence, the code adopted for the simulation of the channel regions and the code that simulates the parasitic regions have been written in two separate Verilog-A modules. A third module describes the overall device and defines, in its structural description part, the channel regions and the parasitic regions that must be instantiated according to the topology of the specific device layout.

When the code has to be adapted to new layouts, the only part that has to be modified is the structural description of the device: it is in this way that the model has been easily applied to different layouts [24] beside the one used for the fully printed OTFTs reported in this work.

IV. VALIDATION AND DISCUSSION

A. MODEL AND CIRCUIT PARAMETERS

The parameters of the VRH model have been estimated with a simultaneous fit of the experimental transfer and output characteristics. These measurements are made in static conditions and, in this case, the presence of parasitic regions in the printed OTFTs, that introduces only "capacitive" effects, does not affect the DC currents. The resulting parameter values are listed in Table 1 and the simulated characteristics are plotted in Fig. 3: as can be seen, despite relying on very few adjustable parameters, the VRH model still provides an acceptable reproduction of the DC behavior over a wide range of drain and gate bias, in above threshold as well as in subthreshold regime.

The gate metallization overlaps the source and drain fingers and introduces overlap capacitances between these terminals. These capacitances have been estimated on the basis of the layout used, giving $C_{gs,ov} = 1.2$ pF and $C_{gd,ov} = 1.8$ pF (the number of source and drain fingers is different), and have been included as discrete elements in the circuit simulation.

B. TRANSIENT SIMULATIONS

As said before, the presence of a coaxial cable to connect M0 with R0 (see Fig. 5) introduces in the circuit a transmission line (RG174). The delay times associated with RG174 are even larger than the intrinsic delay times of the CS amplifier under investigation and are related to the lack of matching of the loads at both ends of the transmission line. Hence, in order to reproduce the experimental measurements, it is necessary to accurately reproduce in the simulations not only the behavior of the CS amplifier, and hence of the OTFT in it, but also the input impedance of the buffer stage. To this end, in the circuit simulations, an accurate SPICE model of the LF412 operational amplifier has been used [20].

In Fig. 6, the experimental transient characteristics of a CS amplifier employing an OTFT with L = 100 μm, W = 400 μm have been precisely fitted in order to have a "fine tuning" of the values of the parasitics present in the circuit, by making small adjustments to the load resistance R0 (from 30 MΩ to 29 MΩ) and to the length of the coaxial cable RG174 (from 30 cm to 32.5 cm). Once the parasitics have been estimated, their values have been kept fixed in all subsequent simulations.

The model is able to precisely simulate the behaviour of the OTFTs used in the CS amplifier as their geometrical dimensions are changed: in fact, as shown in Fig. 6, the output curves obtained using devices with channel lengths ranging from L = 30 μm to L = 400 μm are perfectly reproduced. For an L = 100 μm device it is found that the turn-on and turn-off transients have a rise-time τ_r= 1.8 ms and a fall-time τ_f = 2.7 ms respectively.

In Fig. 7, an OTFT with L = 30 μm, W = 400 μm is used as the active element of the CS amplifier that is operated with different power supply voltages and input pulse signals with different voltage amplitudes (V_{dd} = 10 V, 20 V, and 30 V): the model is able to quantitatively reproduce the output of the amplifier for each of the conditions. In particular, the change of the rise- and fall-time associated with the variation of the power supply voltage (V_{dd}) and the voltage swing of the output signals is correctly reproduced in both the turn-on and turn-off transients (Fig. 7a and Fig. 7b).

It is worth to stress that the results of the simulations reported in Fig. 6 and Fig. 7 have been obtained by changing only the channel length of the OTFT or its bias conditions with no additional tuning of other device parameters: thus the model accurately predicts the dynamic operation of the OTFTs with different geometrical dimensions and under different bias conditions. Hence, this model can be profitably used in a CAD environment during the design steps of a complex circuit.

C. SMALL SIGNAL (CV) SIMULATIONS

The response of the printed OTFTs to small signals (AC analysis) has been studied using the NQS model. The AC simulations, shown in Fig. 3, reproduce qualitatively all the features of the corresponding experimental measurements described in Section II-C. In particular, the decreasing trend of C_p for increasing frequencies, the inflection at $f \sim 10$ kHz and the asymptotic behaviour at high frequency are well reproduced. Moreover, the NQS model can be used to gain

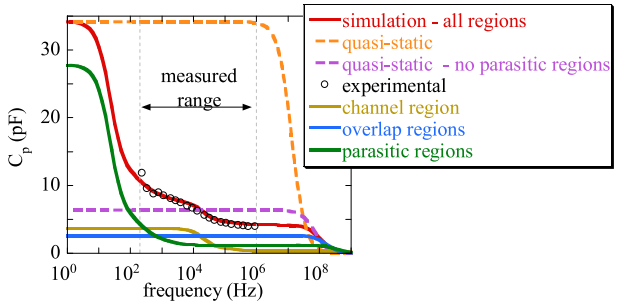

FIGURE 8. C_p vs frequency curves measured (symbols) and simulated (solid lines) using the non-quasi-static model on an L = 100 μm, W = 400 μm device. Contributions to the simulated C_p coming from different device regions have been plotted separately. The simulated C_p vs f curves obtained using quasi-static model including or neglecting the presence of parasitic regions (dashed lines) are also shown.

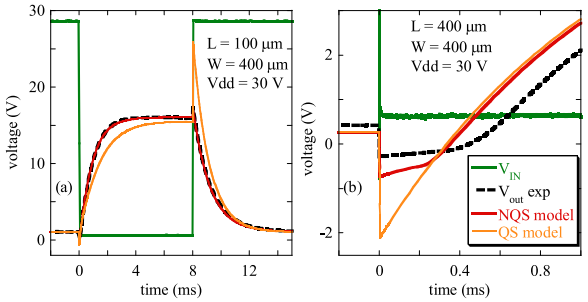

FIGURE 9. Dynamic response of the CS amplifier measured and simulated using the non-quasi-static model and a quasi-static model including the presence of parasitic regions. (a) dynamic response over a whole period of the input signal when an L = 100 μm, W = 400 μm device is used; (b) expanded view of the initial phase of the turn-on transient when an L = 400 μm, W = 400 μm device is used.

some physical insight and valuable indications about possible optimizations of the layout: in Fig. 8, the small signal capacitance measured on the L = 100 μm, W = 400 μm device as a function of f is compared with the corresponding simulation (red curve) made on a frequency range much wider than the range experimentally accessible. The contributions to the simulated C_p coming from different device regions have been plotted separately: as can be seen, the device channel (yellow curve) has an intrinsic cut-off frequency of the order of 10 kHz and, at higher frequencies, it loses the ability to respond to the gate signal. The contribution of the parasitic regions (green curve) is huge but only at very low frequency and determines the rise of C_p in the sub-kilohertz range. For higher frequencies, the carrier dynamics in the parasitic regions, that is dominated by diffusion [25], is not able to follow the gate signal and their contributions to C_p become very small. On the other hand, the contribution of the source and drain overlap regions (blue curve) is present over the whole frequency range.

Hence, the NQS model indicates that, at high frequency, the device dynamic is not very sensitive to the presence of parasitic regions, but they must be taken in account in the design applications operating at low frequencies.

D. NQS VS QS SIMULATION

The possibility to include NQS effects noticeably improves the accuracy of dynamic simulations with respect to QS models.

In Fig. 8 are plotted the Cp-vs-f curves computed by using a QS approach in which the time derivative of the charge distribution is assumed to be zero (LHS of (23)), thus neglecting any delay in the rearrangement of the electrical charge in the device. Two different cases are reported, including or neglecting the presence of parasitic regions: in both cases QS simulations fail to reproduce the frequency dispersion of C_p up to the megahertz range and a very poor agreement with the measured curve is obtained. In particular, the simulation including parasitic regions largely overestimates C_p in the whole frequency range.

In Fig. 9a the QS simulation (including the parasitic regions) of the dynamic response of the CS amplifier is compared with the experimental measurement and with the results obtained by using the NQS model. As can be seen, the QS model overestimates the rise-time of the turn-on transient, due to the exceedingly large value of C_p predicted by this model (see Fig. 8). Moreover, the QS model provides a substantial overestimation of the peak output voltage at the beginning of the turn-off transients, due to the assumption of an instantaneous response of the charge distribution in the device after voltage changes.

In Fig. 9b it is shown an expanded view of the initial phase of the turn-on transient when the L = 400 μm, W = 400 μm device is used in the CS amplifier. The measurement clearly shows the presence of a delay time between the input pulse and the rise of the output signal: this is due to the finite amount of time that the carriers spend to traverse the channel and can be estimated with the well-known text-book formula $\tau_{\text{theo}} = L^2/\mu V_{ds}$. If we use an "effective" mobility $\mu \approx 0.2$ cm^2/Vs and an estimated $V_{ds} \approx 30$ V we correctly guess the order of magnitude of the delay time $\tau_{theo} \approx 0.3$ ms, that compares favourably with the experimental one $\tau_{exp} \approx 0.4$ ms. As can be seen from Fig. 9b, NQS simulations reproduce very well the theoretical delay with $\tau_{sim} \approx 0.28$ ms. On the other hand, the simulation made using the QS model completely lacks any delay in the response and provides a slight overestimation of the (negative) peak output voltage.

V. CONCLUSION

An NQS model particularly well suited for printed OTFTs has been presented and validated with measurements made on devices operated in DC, large-signal and small-signal regimes. The model fully accounts for the peculiar features of printed OTFTs: it is based on the Variable Range Hopping theory, it accounts for Non-Quasi-Static operation and it considers the presence of parasitic regions in the device layout.

It is found that the NQS model is considerably more accurate than the corresponding QS model in the reproduction

of the device dynamic behavior in both large-signal and small-signal operations.

The model has been implemented in Verilog-A and can be profitably used in circuit simulation software environments.

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