3-Way Doherty Power Amplifiers: Design Guidelines and MMIC Implementation at 28 GHz

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***Abstract*— This article presents the design strategy and the implementation of a three-way Doherty power amplifier (DPA3W) to enhance the efficiency at deep power back-off. Theoretical design equations are derived, based on which design charts are drawn to explore the available design space, accounting for practical constraints related to the available technology and selected application. The proposed design strategy is demonstrated by the design, fabrication and experimental characterization of a three-way multistage Doherty amplifier optimized for efficiency peaks at 6 and 12 dB back-off. The amplifier is realized on the WIN Semiconductors 150 nm GaN-SiC high-electron-mobility transistor (HEMT) monolithic process at 28 GHz, targeting 5G applications. The prototype achieves saturated output power in excess of 34 dBm and power added efficiency of the order of 15% from 6 to 12 dB back-off, demonstrating competitive performance and a good agreement between simulations and measurements, thus validating the approach.**

***Index Terms*— Back-off, Doherty, 5G, GaN, high efficiency, monolithic microwave integrated circuit (MMIC), power amplifiers (PAs).**

I. Introduction

THE demand for high capacity of future communication systems forces the adoption of advanced modulation schemes with non-constant envelope and very large peak-to-average-power-ratio (PAPR). This has a strong impact on the transmitter architecture, especially on the power amplifier (PA), which operates in back-off, i.e., at an average power significantly lower than its saturated one.

At sub-6 GHz communication frequencies, different design strategies have been proposed to maintain also in back-off a reasonably high PA efficiency, the most popular one being presently the Doherty PA (DPA) [1], [2], [3], thanks to its relatively simple and robust design, and its good performance in terms of efficiency and linearity over bandwidths compatible with today's standard requirements. Different metrics are currently in use to specify the linearity requirements of the PAs, noise-to-power ratio (NPR) [4] becoming increasingly popular for satellite communications, whereas adjacent channel power ratio (ACPR) and error vector magnitude (EVM) being among the most used for ground communications.

However, 5G applications and beyond would soon require the PA to manage signals with increasing PAPR (9–12 dB), well beyond the classical 6-dB high-efficiency region of standard DPAs. Crest Factor Reduction can be applied, although at the expense of increased complexity and worse linearity [5]. Therefore, architectures to enhance the efficiency at deep power back-off, such as the N-stage and N-way DPA [6], [7], [8], [9], [10], [11], the distributed efficient PA (DEPA) [12], [13], and the sequential-load modulated balanced amplifier (S-LMBA) [14], [15], [16], [17], have been developed.

The DPA and S-LMBA architectures typically rely on a limited number of active devices (usually three, one for the Main and two for the Auxiliary), but they are particularly affected by a strong gain penalty, due to the asymmetric input power splitting and the class-C bias point adopted for the Auxiliary devices [6], [9], [17]. Optimized operations in terms of achievable gain and efficiency are possible but require multi-RF-inputs [7], [10]. On the other side, the DEPA has a somewhat limited gain penalty but needs an increasingly high number of active devices to optimize the efficiency at a deeper output power back-off (OBO) [12], [13]. In addition, the DEPA and S-LMBA eliminate the load modulation of the Main, thus favoring wideband operation, but at the cost of overdriving it over the whole high-efficiency region, with unavoidable reliability and stress issues. The Main overdriving issue is also present in some of the N-stage and N-way DPAs proposed in literature [6], [7], [9], being based on output combiners that hamper the modulation of the Main load when more than one auxiliary stage is on. A viable solution for this limiting factor has been proposed in [18] and [19] and implemented at 2.65 GHz in [8]. In the latter, the novel output combiner scheme was exploited in conjunction with gate envelope tracking to mitigate the low load modulation due to the deep class-C bias of the auxiliary stages.

In general, most of the above-mentioned solutions are currently limited to single-stage hybrid demonstrators, with excellent efficiency but a limited gain (typically around 10 dB), and often complex architectures, limiting so far their adoption at higher communications frequencies, where PA architectures with one or more driver stages are inevitably called for.

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Recently, 6 dB DPAs and LMBAs are starting to appear at Ka-band and 5G FR2 frequencies with competitive performance [20], [21], [22], [23], despite the need of multistage architectures. Therefore, this work aims at exploring the feasibility of deep-OBO DPAs at similar frequencies and their convenience as compared to more classical solutions with a less severe gain penalty.

Concerning these DPAs, the nomenclature is not unique; in this work, N-stage indicates $N-1$ drivers and a final power stage, whereas M-way refers to a DPA with M efficiency peaks, and hence with $M-1$ auxiliary devices.

In the following, a step-by-step design strategy for three-way DPAs (DPA3W) based on the combiner of [18] and [19] is provided. The complete design flow for the computation of the combiner's parameters as well as the devices' selection is presented, critically discussing the possible trade-offs and introducing general design charts to visualize the available design space when accounting for several technology constraints.

The approach is validated by the design and experimental characterization of a demonstrator targeting the FR2 5G band n261 (27.5–28.35 GHz), optimized at 6 and 12 dB OBO. The prototype, manufactured in the 150 nm GaN-SiC high-electron-mobility transistor (HEMT) process of WIN Semiconductors is, to the best of the authors' knowledge, the first monolithic microwave integrated circuit (MMIC) DPA3W. It compares well with the present state of the art at similar frequencies, demonstrating the validity of the approach and opening to the adoption of this strategy also for mm-wave applications.

This article is structured as follows. Section II reports the theoretical foundations and derives the design equations for a generic DPA3W, exploring the design space and the available degrees of freedom with the aid of graphical charts. In Section III, the theoretical formulation is applied to the design of an MMIC three-stage DPA3W demonstrator in GaN technology at 28 GHz. The experimental characterization results of the manufactured MMIC are presented in Section IV. Finally, conclusions are drawn in Section V.

II. Theoretical Analysis

The proposed DPA3W architecture of Fig. 1(a) can synthesize the efficiency profile shown in Fig. 1(b) provided that the active devices are driven to generate current profiles like those of Fig. 1(c) and corresponding voltage response similar to those of Fig. 1(d). The two back-off efficiency peaks occur at a distance (in dB) OBO_2 and OBO from saturation. Assuming the simplified ideal behavior of the active devices, the following operating regions can be identified, relative to the normalized dynamic range (i.e., the driving input voltage) x (where $0 \le x \le 1$).

1) $0 \le x < x_1$ *(Low Power Region):* Only the Main (M) device is conducting with a fixed load condition Z_{M}, while the two Auxiliary devices (A_1 and A_2) are OFF, assumed as open circuits. Hence, the impedance Z_{w} results in an open circuit, and the Main sees only the series of the $\lambda/4$ transmission line (TL) Z_1 and R_{L}.

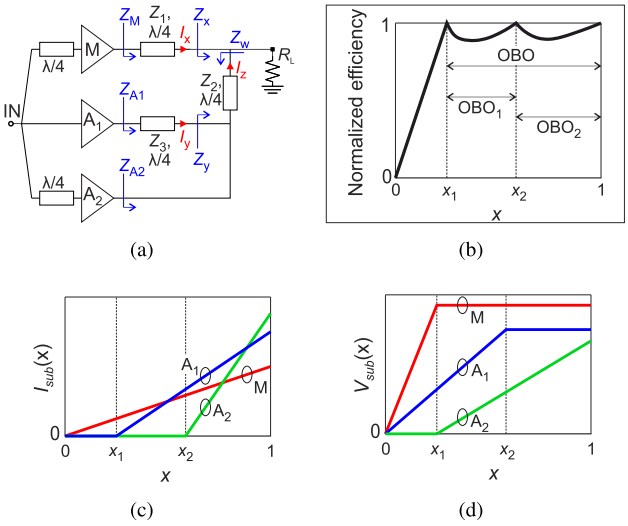

Fig. 1. Proposed structure (a) for a DPA3W with (b) resulting efficiency, and typical profiles of (c) current and (d) voltage of the three devices.

2) $x_1 \le x < x_2$ *(OBO_1 Region):* At the first break point $x = x_1$, M achieves its maximum voltage swing (voltage saturation) and A_1 turns on, modulating Z_{M}, while A_2 is still off. The current provided by A_1 increases the impedance Z_{x}, and the $\lambda/4$ TL Z_1 acts as an impedance inverting network, thus decreasing the value of Z_{M}.
3) $x_2 \le x \le 1$ *(OBO_2 Region):* At the second break point $x = x_2$, A_1 reaches its maximum voltage swing (voltage saturation), and A_2 turns on, modulating both Z_{M} and Z_{A_1}. Indeed, the current injected by A_2 increases the impedance Z_{y}, and the $\lambda/4$ TL Z_3 acts as an impedance inverting network for A_1, thus decreasing the value of Z_{A_1}. Simultaneously, the currents of A_1 and A_2 further increase Z_{x}, thus decreasing the impedance Z_{M}. At $x = 1$ all devices are in saturation, i.e., operate with maximum current and voltage swings.

At the input of the DPA3W, an *ad hoc* splitter is clearly required to properly compensate the phase shifts introduced by the $\lambda/4$ TLs of the output combiner, as well as appropriately dividing the input power among the three amplifying branches, thus leading to the final architecture reported in Fig. 1(a).

The fundamental components of the drain current and voltage of each device are indicated as $I_{\mathrm{sub}}(x)$ and $V_{\mathrm{sub}}(x)$, respectively, where sub corresponds to M, A_1 and A_2 for the Main, and the two Auxiliary devices, respectively.

The maximum voltage (peak value) for each device is

$$V_{\mathrm{Max,sub}} = V_{\mathrm{DD,sub}} - V_{\mathrm{k,sub}} \tag{1}$$

where the supply ($V_{\mathrm{DD,sub}}$) and knee ($V_{\mathrm{k,sub}}$) voltages can in general be different among the stages. Therefore, it is useful to define the normalization coefficient

$$\beta_n = \frac{V_{\mathrm{Max,A}_n}}{V_{\mathrm{Max,M}}} \qquad n = 1, 2. \tag{2}$$

Similarly, the maximum current (peak value) of each device will be indicated in the following as $I_{\mathrm{Max,sub}}$. Its relation with the fundamental current component at saturation [$I_{\mathrm{sub}}(1)$]

depends on the bias point of the device, i.e., its quiescent current $I_{\mathrm{DQ,sub}}$. By defining the normalized quiescent current $\xi_{\mathrm{sub}} = I_{\mathrm{DQ,sub}}/I_{\mathrm{Max,sub}}$, the relation with the peak fundamental current is

$$I_{\mathrm{Max,sub}} = \frac{I_{\mathrm{sub}}(1)}{I_1(\xi_{\mathrm{sub}}, 1)} \tag{3}$$

where $I_1(\xi, x)$ is the coefficient of the fundamental component of a truncated (normalized) sinusoidal waveform given by [18], [24]

$$I_1(\xi, x) = \frac{x}{2\pi} \cdot \frac{\theta_x - \sin(\theta_x)}{1 - \cos\left(\frac{\theta_x}{2}\right)} \tag{4}$$

$$\theta_x = \begin{cases} 0, & \text{if } \xi \le 0,\ x < \left|\frac{\xi}{1-\xi}\right| \\ 2\pi, & \text{if } \xi \ge 0,\ x < \left|\frac{\xi}{1-\xi}\right| \\ 2 \cdot \arccos\left(\frac{\xi}{x \cdot (\xi - 1)}\right), & \text{otherwise.} \end{cases} \tag{5}$$

Since all circuit elements are assumed to be lossless, the output power of the DPA3W is given by the sum of the output powers of the three devices

$$P_{\mathrm{DPA}}(x) = P_{\mathrm{M}}(x) + P_{\mathrm{A_1}}(x) + P_{\mathrm{A_2}}(x) \tag{6}$$

where

$$P_{\mathrm{sub}}(x) = \frac{1}{2} \cdot V_{\mathrm{sub}}(x) \cdot I_{\mathrm{sub}}(x). \tag{7}$$

The design relationships for the proposed DPA3W are derived by assuming as design goals the position of the efficiency peaks (x_1 and x_2) and the target output power at saturation [$P_{\mathrm{DPA,sat}} = P_{\mathrm{DPA}}(1)$], and as free parameters the common-node resistance R_{L} and the bias point of the Main, expressed in terms of drain voltage $V_{\mathrm{DD,M}}$ and quiescent current $I_{\mathrm{DQ,M}}$. The characteristic impedances of the $\lambda/4$ TLs of the output combiner (Z_1, Z_2, Z_3), the bias points of $\mathrm{A_1}$ and $\mathrm{A_2}$, and the maximum currents of all devices ($I_{\mathrm{Max,M}}$, $I_{\mathrm{Max,A_1}}$, $I_{\mathrm{Max,A_2}}$) are derived accordingly. Note that in the following the 90° phase rotation in any relation across a $\lambda/4$ TL is omitted since all quantities represent the magnitude of the corresponding phasors. In other words, it is assumed that the phase of the branch signals is such as to ensure in-phase current summation at the common node (i.e., into R_{L}).

A. Derivation of the Combiner's Parameters

With reference to Fig. 1(a) and accounting for the constitutive equation of a $\lambda/4$ TL at center frequency [25], it follows that I_{x} is constant for $x_1 \le x \le 1$. Thus, the following relevant parameters can be derived:

$$\alpha_1^2 = \frac{P_{\mathrm{DPA}}(x_1)}{P_{\mathrm{DPA}}(1)} = \frac{\frac{1}{2}R_{\mathrm{L}}I_{\mathrm{x}}^2(1)}{\frac{1}{2}R_{\mathrm{L}}[I_{\mathrm{x}}(1) + I_{\mathrm{z}}(1)]^2} = \frac{I_{\mathrm{x}}^2(1)}{[I_{\mathrm{x}}(1) + I_{\mathrm{z}}(1)]^2} \tag{8}$$

$$\alpha_2^2 = \frac{P_{\mathrm{DPA}}(x_2)}{P_{\mathrm{DPA}}(1)} = \frac{\frac{1}{2}R_{\mathrm{L}}[I_{\mathrm{x}}(1) + I_{\mathrm{z}}(x_2)]^2}{\frac{1}{2}R_{\mathrm{L}}[I_{\mathrm{x}}(1) + I_{\mathrm{z}}(1)]^2} = \frac{[I_{\mathrm{x}}(1) + I_{\mathrm{z}}(x_2)]^2}{[I_{\mathrm{x}}(1) + I_{\mathrm{z}}(1)]^2} \tag{9}$$

which, accounting for the generic definition of $\mathrm{OBO} = -10\log_{10} P_{\mathrm{DPA}}(x)/P_{\mathrm{DPA}}(1)$, are also given by

$$\alpha_1 = 10^{-(\mathrm{OBO}/20)} \tag{10a}$$

$$\alpha_2 = 10^{-(\mathrm{OBO_2}/20)} \tag{10b}$$

where OBO and $\mathrm{OBO_2}$ are design goals. By combining (8) and (9), one finds a relation between the overall current coming from the Auxiliary branches (I_{z}) and the one of the Main (I_{x}), at x_2 and saturation

$$I_{\mathrm{z}}(x_2) = I_{\mathrm{x}}(x_2)\frac{\alpha_2 - \alpha_1}{\alpha_1} \tag{11}$$

$$I_{\mathrm{z}}(1) = I_{\mathrm{x}}(1)\frac{1 - \alpha_1}{\alpha_1}. \tag{12}$$

Adopting (8) and (12), $I_{\mathrm{x}}(1)$ can be expressed as function of R_{L} and $P_{\mathrm{DPA,sat}}$

$$I_{\mathrm{x}}(1) = \alpha_1 \cdot \sqrt{\frac{2 \cdot P_{\mathrm{DPA,sat}}}{R_{\mathrm{L}}}}. \tag{13}$$

Since M achieves voltage saturation at x_1, $V_{\mathrm{Max,M}}$ is constant for $x_1 \le x \le 1$, which implies constant I_{x}. The characteristic impedance of the $\lambda/4$ TL in front of M can be derived from (13)

$$Z_1 = \frac{V_{\mathrm{Max,M}}}{I_{\mathrm{x}}(1)} = \frac{V_{\mathrm{Max,M}}}{\alpha_1} \cdot \sqrt{\frac{R_{\mathrm{L}}}{2 \cdot P_{\mathrm{DPA,sat}}}}. \tag{14}$$

Similarly, the characteristic impedance of the $\lambda/4$ TL in front of $\mathrm{A_2}$ can be derived by using (12) and (13)

$$Z_2 = \frac{V_{\mathrm{Max,A_2}}}{I_{\mathrm{z}}(1)} = \frac{\beta_2 \cdot V_{\mathrm{Max,M}}}{1 - \alpha_1} \cdot \sqrt{\frac{R_{\mathrm{L}}}{2 \cdot P_{\mathrm{DPA,sat}}}} \tag{15}$$

whereas, considering that

$$I_{\mathrm{y}}(x_2) = \frac{V_{\mathrm{L}}(x_2)}{Z_2} = \frac{R_{\mathrm{L}} \cdot [I_{\mathrm{x}}(x_2) + I_{\mathrm{z}}(x_2)]}{Z_2} \tag{16}$$

and by using (11), (13), and (15), the characteristic impedance of the $\lambda/4$ TL in front of $\mathrm{A_1}$ results

$$Z_3 = \frac{V_{\mathrm{Max,A_1}}}{I_{\mathrm{y}}(x_2)} = \frac{\beta_1 \cdot \beta_2 \cdot V_{\mathrm{Max,M}}^2}{2 \cdot \alpha_2(1 - \alpha_1) \cdot P_{\mathrm{DPA,sat}}}. \tag{17}$$

Notably, (14), (15), and (17) allow the synthesis of the output combiner once the values of OBO, $\mathrm{OBO_2}$, and $P_{\mathrm{DPA,sat}}$ are chosen.

B. Derivation of the Active Devices' Parameters

To complete the synthesis of the output section of the DPA3W, it is necessary to estimate the maximum current required by each device, and thus their active periphery. This can be accomplished deriving first their fundamental component at saturation $I_{\mathrm{sub}}(1)$ and then the associated maximum current $I_{\mathrm{Max,sub}}$ by using (3)–(5). Exploiting the $\lambda/4$ TL

properties, Kirchoff current law (KCL) at $x = 1$, and (14)–(6), one finds

$$I_{\mathrm{M}}(1) = \frac{V_{\mathrm{L}}(1)}{Z_1} = \frac{R_{\mathrm{L}}[I_{\mathrm{x}}(1) + I_{\mathrm{z}}(1)]}{Z_1} = \alpha_1 \frac{2P_{\mathrm{DPA,sat}}}{V_{\mathrm{Max,M}}} \quad (18)$$

$$I_{\mathrm{A1}}(1) = \frac{V_{\mathrm{Max,A2}}}{Z_3} = \frac{\alpha_2(1-\alpha_1)}{\beta_1} \cdot \frac{2P_{\mathrm{DPA,sat}}}{V_{\mathrm{Max,M}}} \quad (19)$$

$$I_{\mathrm{A2}}(1) = 2\frac{P_{\mathrm{A_2,sat}}}{V_{\mathrm{Max,A2}}} = \frac{(1-\alpha_1-\alpha_2+\alpha_1\alpha_2)}{\beta_2} \cdot \frac{2P_{\mathrm{DPA,sat}}}{V_{\mathrm{Max,M}}}. \quad (20)$$

It is worth noting that the fundamental current components do not depend on R_{L}, confirming that the latter can be used as a free parameter to widen the design space, i.e., increase the feasibility of the characteristic impedances of the $\lambda/4$ TLs given by (14)–(17), in the selected technology.

Assuming the bias condition of M as a free parameter, its $I_{\mathrm{Max,M}}$ can be derived by substituting (18) in (3) and exploiting (4) and (5)

$$I_{\mathrm{Max,M}} = \frac{I_{\mathrm{M}}(1)}{I_1(\xi_{\mathrm{M}}, 1)} = \frac{2 \cdot \alpha_1 \cdot P_{\mathrm{DPA,sat}}}{V_{\mathrm{Max,M}} \cdot I_1(\xi_{\mathrm{M}}, 1)}. \quad (21)$$

The maximum current of the Auxiliary devices can be derived by combining (19), (20), (18), and (3)-(5)

$$I_{\mathrm{Max,A_1}} = \frac{1}{\beta_1} \cdot I_{\mathrm{Max,M}} \cdot \frac{I_1(\xi_{\mathrm{M}}, 1)}{I_1(\xi_{\mathrm{A_1}}, 1)} \cdot \frac{\alpha_2}{\alpha_1} \cdot (1-\alpha_1) \quad (22a)$$

$$I_{\mathrm{Max,A_2}} = \frac{\beta_1}{\beta_2} \cdot I_{\mathrm{Max,A_1}} \cdot \frac{I_1(\xi_{\mathrm{A_1}}, 1)}{I_1(\xi_{\mathrm{A_2}}, 1)} \cdot \left(\frac{1}{\alpha_2} - 1\right). \quad (22b)$$

To ensure the proper turn-on of the Auxiliary devices, it is possible to compute their virtual negative bias point ξ_{A_n} as

$$\xi_{\mathrm{A}_n} = \frac{x_n}{x_n - 1}, \qquad n = 1, 2 \quad (23)$$

being the breakpoints x_n the solutions of the following equation [24]:

$$I_1(\xi_{\mathrm{M}}, x_n) - \alpha_n \cdot I_1(\xi_{\mathrm{M}}, 1) = 0 \quad (24)$$

which defines the linear current profile of the Main device.

Finally, the impedance at the current generator plane of each device is $Z_{d_i,\mathrm{sub}} = V_{\mathrm{sub}}/I_{\mathrm{sub}}$ [which coincides with Z_{sub} in Fig. 1(a)], whereas their optimum load resistance is given by

$$R_{\mathrm{opt,sub}} = 2 \cdot V_{\mathrm{Max,sub}}/I_{\mathrm{Max,sub}}. \quad (25)$$

A summary of the design procedure is provided in the flowchart of Fig. 2. It is worth mentioning that the combiner topology and the corresponding system of equations reported above can be easily extended to the case of DPAs with more than two efficiency peaks, i.e., more than two Auxiliary devices.

C. Feasibility Analysis and Design Space

The design procedure laid out up to now and summarized in Fig. 2 has no theoretical limitations and could be applied to synthesize, on paper, any M-way Doherty architecture having an arbitrary position of the efficiency peaks, saturated output power, operating frequency, etc. However, as usual, theory has

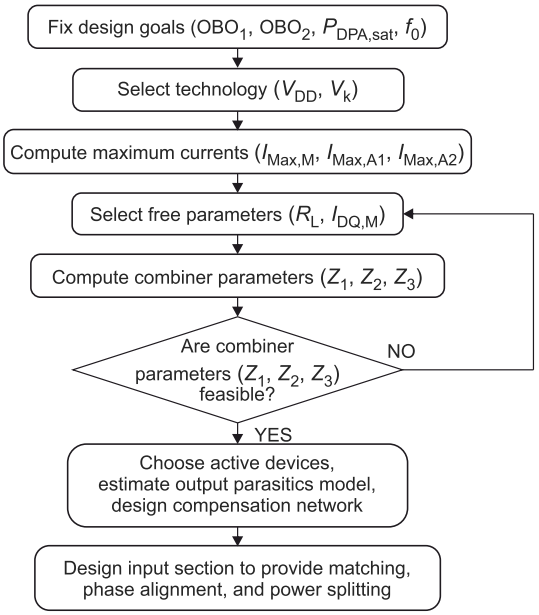

Fig. 2. Flowchart of the design procedure for a DPA3W.

to meet technology constraints to produce feasible designs. Considering MMIC technologies, once the DPA3W design goals are fixed, the main limitations associated with passive and active components are the feasibility of the characteristic impedances of the $\lambda/4$ TLs (Z_1, Z_2, and Z_3) and the maximum allowable current and voltage swings. Characteristic impedances can be considered feasible if included in the range 20–100 Ω, almost independently of the specific technology. The maximum current and voltage swings, instead, are heavily affected by the semiconductor proprieties of the specific technologies. This leads to the identification of the active devices macro parameters such as current density, drain bias, knee, and breakdown voltages. Focusing on GaN technology for mm-wave applications (i.e., with a gate length of the order of 0.1–0.15 μm), the current density typically ranges within 400–1000 mA/mm, whereas recommended drain bias voltages are within 10–30 V. Both features, together with the corresponding knee voltage value, concur to determine the achievable output power from a chosen device.

Accounting for these considerations, design charts are provided in Fig. 3 to aid the designer to visualize the contrasting constraints that influence the DPA3W design space. In particular, the contours of Z_i as functions of $P_{\mathrm{DPA,sat}}$ and R_{L} are reported, fixing the design goals to OBO = 12 dB and $\mathrm{OBO_2}$ = 6 dB. Moreover, despite the developed theory allows to account for different drain bias voltage of the devices, in these charts only the cases with $V_{\mathrm{Max},M} = V_{\mathrm{Max,A_1}} = V_{\mathrm{Max,A_2}} = 16$ V [see Fig. 3(a)–(c)] and 8 V [see Fig. 3(d)–(f)] are reported, leaving to the readers the possibility to explore larger design spaces by accounting for different values of OBOs and $V_{\mathrm{Max,sub}}$.

The available space for each parameter is highlighted in the corresponding plots with shaded areas, whose intersection represents the overall design space, considering the output power as design goal. In the first case, i.e., $V_{\mathrm{Max,M,A_1,A_2}} = 16$ for

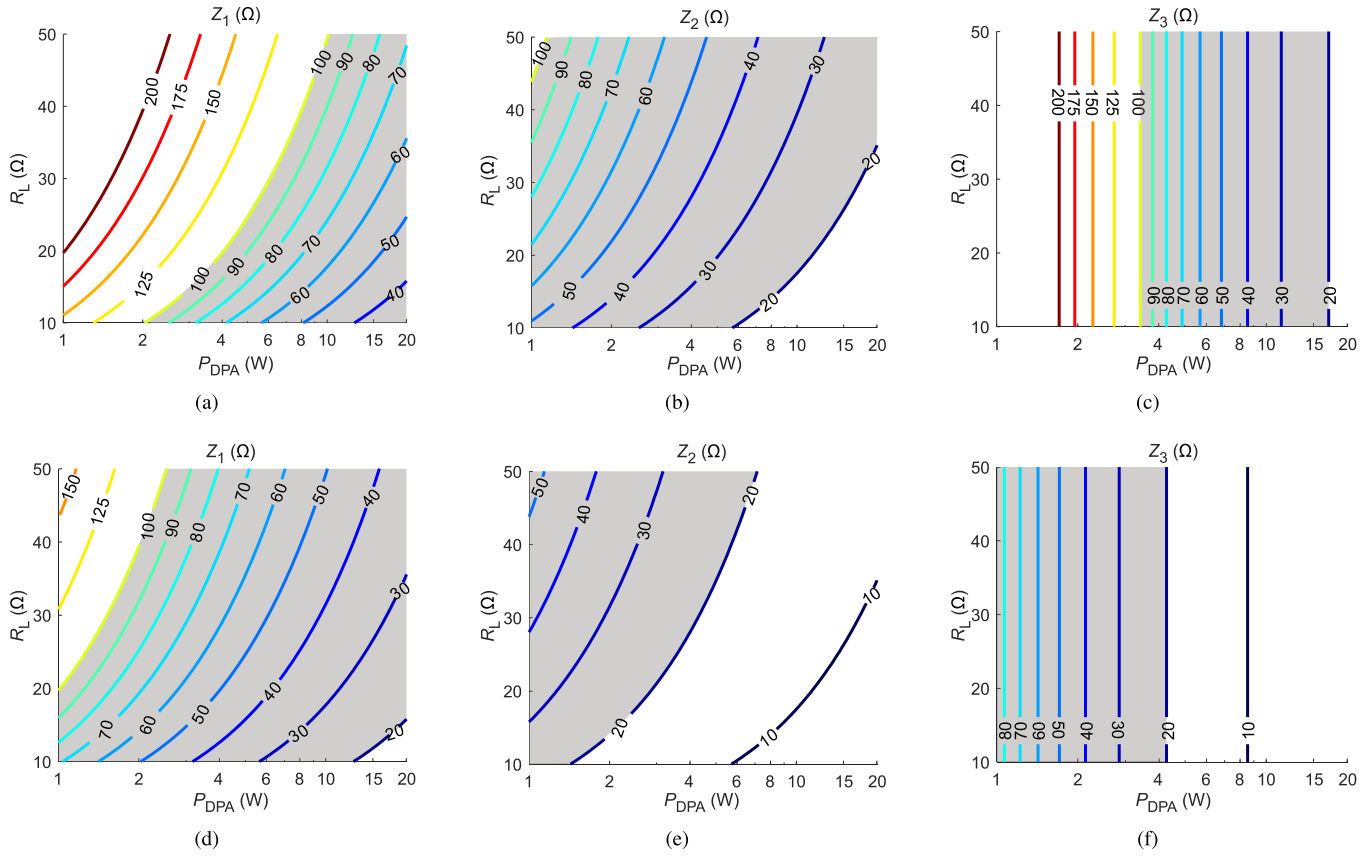

Fig. 3. Design charts for the characteristic impedances Z_1, Z_2, Z_3 of the combiner, with OBO = 12 dB and OBO_2 = 6 dB, $V_{Max,M} = V_{Max,x_1} = V_{Max,A_2} = V_{Max,sub}$ (a)–(c) for $V_{Max,sub}$ = 16 V and (d)–(f) for $V_{Max,sub}$ = 8 V. The shaded areas correspond to the available design space, dictated by feasible characteristic impedances (20 Ω ≤ Z_i ≤ 100 Ω).

$R_L = 50$ Ω, the resulting Z_1, would be practically unfeasible for any value of $P_{DPA,sat} \leq 10$ W. On the contrary, Z_2 is always feasible and does not pose any constraint, whereas Z_3 only depends on $P_{DPA,sat}$ and becomes feasible for relatively high power values, above 3 W. Anyway, if a $P_{DPA,sat} \leq 10$ W is required, the designer can select a lower value for the free parameter R_L to accommodate such a need, at the expense of an additional post-matching network (PMN) (which inevitably impacts on area, losses, complexity). For instance, an output power of about 5 W can be achieved by setting $R_L = 20$ Ω which leads to more practical and feasible values of the output combiner impedances. However, Fig. 3(a)–(c) also show that $P_{DPA,sat} \lessapprox 4$ W is not achievable with $V_{Max,M,A_1,A_2} = 16$ V due to the limitation on Z_3. To design a DPA3W with OBO = 12 dB and OBO_2 = 6 dB and targeting relatively low output power, the designer has to play with the voltage swing across the devices in order to land on a feasible output combiner. For instance, Fig. 3(d)–(f) show the design charts for $V_{Max,M} = V_{Max,A_1} = V_{Max,A_2} = 8$ V. Notably, all the impedances become feasible and well inside the practical limits of 20–100 Ω for any $P_{DPA,sat} \leq 4$ W, confirming both versatility and feasibility of the proposed architecture.

III. Design

In this work, the 150 nm gate length GaN-SiC HEMT process by WIN Semiconductors is adopted to design a 3 W DPA3W for 5G applications around 28 GHz, optimized at 6 and 12 dB OBO. The normalized fundamental current, voltage, and impedance profiles for such an architecture assuming $V_{Max,M} = V_{Max,A_1} = V_{Max,A_2} = V_{Max,sub}$ are reported in Fig. 4. Notably, the maximum current of the Auxiliary devices is 1.5 times higher than that of the Main. Therefore, either the Auxiliary devices will have a larger periphery, or the Main device will be under-utilized if three identical devices were to be used.

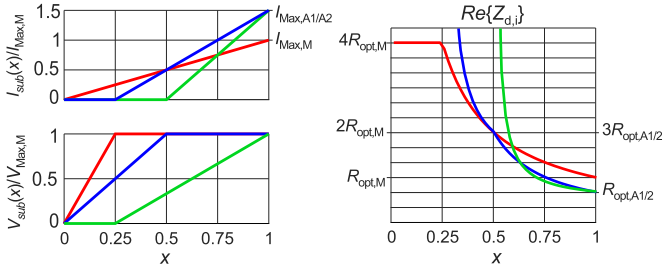

Fig. 4. Currents, voltages and impedances profiles for a 6/12 dB OBO DPA3W.

A. DPA3W Assessment in the Selected Technology

The selected technology has operating voltage $V_{DD} = 20$ V, current density around 400–500 mA/mm, and a scalable

non-linear model for the active devices. The knee voltage is estimated to be $V_{\rm k} = 4$ V, leading to $V_{\rm Max,sub} \leq 16$ V. Despite the developed theory allows to account for the different bias conditions of the devices, the combiner design is here carried out based on a class-B approximation for all the devices, which can be considered sufficiently accurate. Therefore, (4) reduces to $I_1(x) = x$, which implies $I_{\rm Max,sub} = 2 \cdot I_{\rm sub}$(1). Following the flowchart of Fig. 2, the design charts of Fig. 3(a)–(c), and the considerations made on the technology constraints, $R_{\rm L}$ is set to =11.3 Ω, which represents a reasonable trade-off between feasibility and complexity of the combiner. The parameters computed according to (14)–(17), and the corresponding maximum currents given by (21) and (22), result

$$Z_1 = 81\ \Omega \quad I_{\rm Max,M} = 110\ {\rm mA}$$
$$Z_2 = 27\ \Omega \quad I_{\rm Max,A1} = 164\ {\rm mA}$$
$$Z_3 = 97\ \Omega \quad I_{\rm Max,A2} = 164\ {\rm mA}.$$

Active devices, for which the foundry non-linear model is validated, suitable to provide the required currents are $4 \times 75\,\mu$m for the Main and $6 \times 100\,\mu$m for each of the Auxiliary devices. Their output parasitics model in the 27–29 GHz band is a shunt $C_{\rm o,sub}$-series $L_{\rm o,sub}$, as shown in Fig. 5.

A shunt $L_{\rm c,sub}$ compensation of the reactance is possible, but it brings about a change of the resistance, i.e., a scaling of currents and voltages, from the combiner plane (C) to the intrinsic drain plane ($D_{\rm i}$) highlighted in Fig. 5. Therefore, a recomputation of the combiner parameters is required. A more complex compensation strategy that does not modify the impedance levels is in theory possible, but it is avoided here due to the complexity and losses at this frequency. The values of the output parasitics and corresponding compensation elements are

$$C_{\rm o,M} = 125\ {\rm fF} \quad C_{\rm o,A1/A2} = 230\ {\rm fF}$$
$$L_{\rm o,M} = 36\ {\rm pH} \quad L_{\rm o,A1/A2} = 30\ {\rm pH}$$
$$L_{\rm c,M} = 225\,{\rm pH} \quad L_{\rm c,A1/A2} = 111\ {\rm pH}.$$

The voltages scale from $V_{\rm Max,sub} = V_{\rm DD} - V_{\rm k} = 16$ V for all devices at plane $D_{\rm i}$ to $V'_{\rm Max,M} = 13.8$ V and $V'_{\rm Max,A1/A2} = 12.6$ V at plane C, due to the different parasitic and compensation networks. Therefore, the recomputed combiner parameters and maximum currents become

$$Z'_1 = 70\ \Omega \quad I'_{\rm Max,M} = 128\ {\rm mA}$$
$$Z'_2 = 21\ \Omega \quad I'_{\rm Max,A1} = 208\ {\rm mA}$$
$$Z'_3 = 61\,\Omega \quad I'_{\rm Max,A2} = 208\ {\rm mA}.$$

Indeed, comparing the initial set of parameters with the final one, one can easily note that the characteristic impedances become more suitable for an MMIC implementation while the current values vary only slightly, and are still achievable with the formerly selected devices, i.e., the $4 \times 75\,\mu$m for the Main and the $6 \times 100\,\mu$m for each of the Auxiliary devices.

The optimum loads of the devices, computed according to (25) at plane $D_{\rm i}$, are $R_{\rm opt,M} = 145\ \Omega$ and $R_{\rm opt,A_1} = R_{\rm opt,A_2} = 97\ \Omega$.

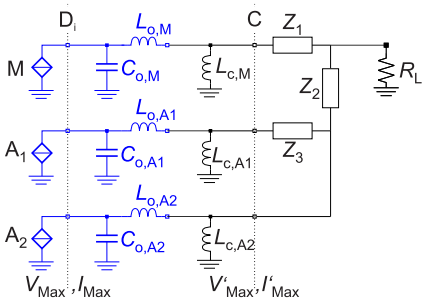

Fig. 5. Schematic of the DPA output combiner implemented with ideal TLs, where the transistors are represented as current sources with CL parasitics, resonated out by means of a shunt L.

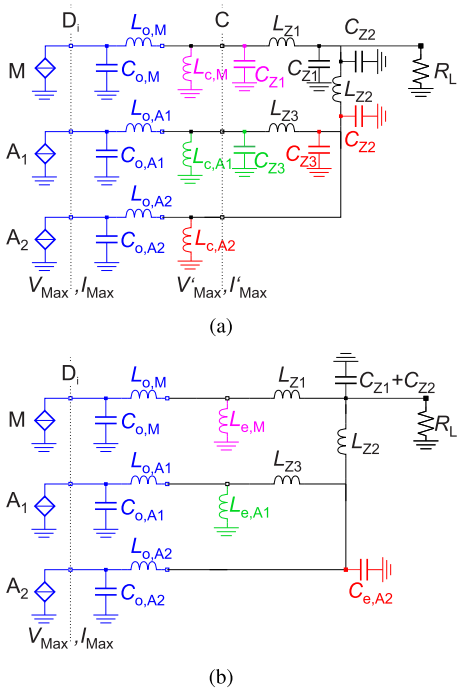

Fig. 6. Schematic of the DPA output combiner, where the transistors are represented as current sources with CL parasitics, resonated out by means of a shunt L (a) where each TL is implemented with a lumped π equivalent and (b) with a minimum number of elements.

B. Output Combiner Implementation

The output combiner is implemented in lumped form, replacing each $\lambda/4$ TL section with its π CLC equivalent network derived at $f_0 = 28$ GHz [see Fig. 6(a)]. The resulting C and L, derived according to $C_{Zi} = 1/(2\pi f_0 Z_i)$ and $L_{Zi} = Z_i/(2\pi f_0)$, are given in Table I. This implementation, together with the choice of compensating the device parasitics by means of a simple shunt inductive element, allows to minimize the number of circuit components, thus also complexity and losses. In fact, as shown in Fig. 6(a) and (b), the elements connected to the same node (highlighted in the same color) are merged into one equivalent reactive element, which results inductive on the M and A1 branches ($L_{\rm e,M}$, $L_{\rm e,A1}$), and capacitive on the A2 branch ($C_{\rm e,A2}$).

The real-to-real PMN from $R_{\rm L} = 11.3$ to 50 Ω is implemented by means of two $\lambda/4$ TL sections, also implemented in lumped form.

TABLE I
CIRCUIT PARAMETERS OF THE OUTPUT COMBINER

C_{Z1} [fF]	L_{Z1} [pH]	C_{Z2} [fF]	L_{Z2} [pH]	C_{Z3} [fF]	L_{Z3} [pH]	$L_{e,M}$ [pH]	$L_{e,A1}$ [pH]	$C_{e,A2}$ [fF]
82	396	265	122	93	346	523	396	68

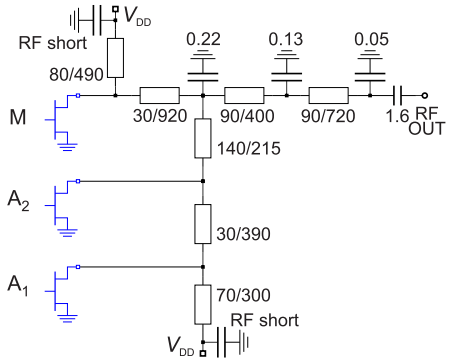

Fig. 7. Schematic of the output combiner of the DPA3W implemented in MMIC technology. Microstrip dimensions are specified as width/length (in μm) and capacitor values are in pF.

The resulting schematic of the DPA3W output section, translated into real circuit elements available in the selected MMIC process (where inductors are replaced by TLs due to layout as well as current handling issues) and optimized around 28 GHz, is shown in Fig. 7, where the output equivalent model of the transistors has been replaced by the full symbol (in blue). The optimization goals impose a trade-off between correct load modulation [as identified in Fig. 4 (right)] and limited losses (within -1.5 dB) across the whole dynamic range (i.e., at $x = x_1, x_2, n1$). Note that, in the synthesized architecture, the position of A_1 and A_2 is swapped for layout convenience. Also, the shunt capacitor $C_{e,A2}$ has resulted unnecessary during the optimization and has therefore been removed. The simulated load modulation and losses, adopting as device model ideal current sources with LC parasitics, are shown in Fig. 8. According to Fig. 8(a)–(c), all the devices maintain the correct load modulation, nearly on the real axis at f_0, and reasonably close to it from 27.5 to 28.5 GHz. The power losses (both mismatch and ohmic) are maintained within the targeted range across the whole high-efficiency region, and are lower at saturation than at the back-off points.

C. Two-Stage DPA3W Architecture

Simulated power sweeps of the 4 $\times$ 75 μm and 6 $\times$ 100 μm devices at 28 GHz return power gain and peak efficiency around 10 dB and 55%, respectively, for a class-AB bias (100 mA/mm) on the optimum load.

Given the input power splitting factors required to synthesize the current profiles of Fig. 4 with the selected devices, a single-stage DPA3W architecture results unfeasible. The insertion of a driver in each of the branches is needed to ensure sufficient gain. Drivers able to correctly drive the corresponding final stage are, respectively, the 2 $\times$ 100 μm for the Main and 4 $\times$ 75 μm for the Auxiliary stages.

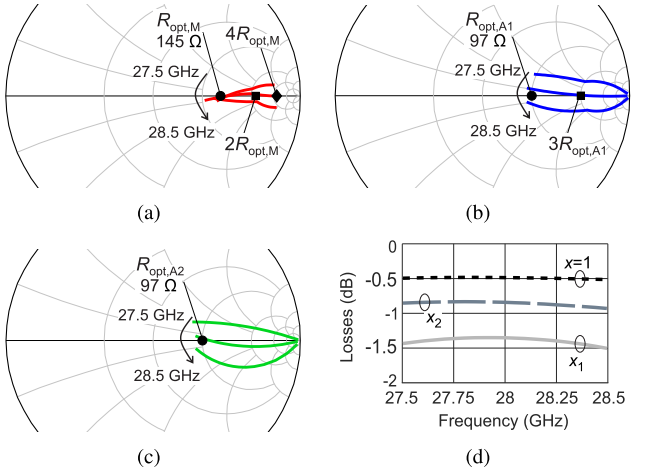

Fig. 8. Simulated (a)–(c) load modulation at the intrinsic drain plane (D_i) of the three power devices and (d) losses of the output section (combiner and PMN) of Fig. 7.

TABLE II
CIRCUIT PARAMETERS OF THE STABILIZATION NETWORKS

Device Periphery [μm]	$R_{stab,1}$ [Ω]	C_{stab} [pF]	$R_{stab,2}$ [Ω]	L_{stab} [pH]
2×100	13	2.3	2.7	75
4×75	18	3.3	2.8	60
6×100	12	3.5	1.8	70

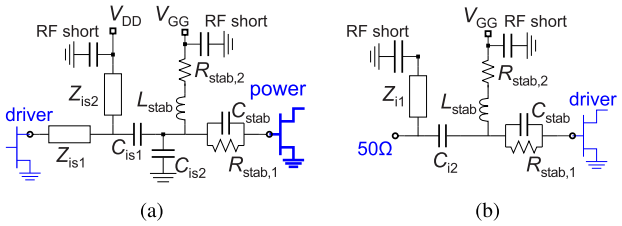

Fig. 9. Schematics of (a) ISMN and (b) IMN topologies, including the input stabilization network of the corresponding devices.

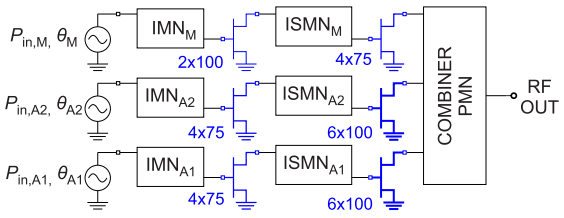

Fig. 10. Schematic of the two-stage DPA3W with three separate RF inputs.

All devices are stabilized in and out of the band by means of a series $R_{stab,1} \parallel C_{stab}$ network and a shunt $R_{stab,2}$-L_{stab} (which will be implemented as an inductive stub), whose values are reported in Table II.

The interstage (IS) and input (I) matching networks (MNs) are designed to minimize reflections, thus maximizing the power transfer along the transistor chain. The ISMNs transform the input impedance of the stabilized power devices into the optimum load of the drivers, whereas the IMNs transform

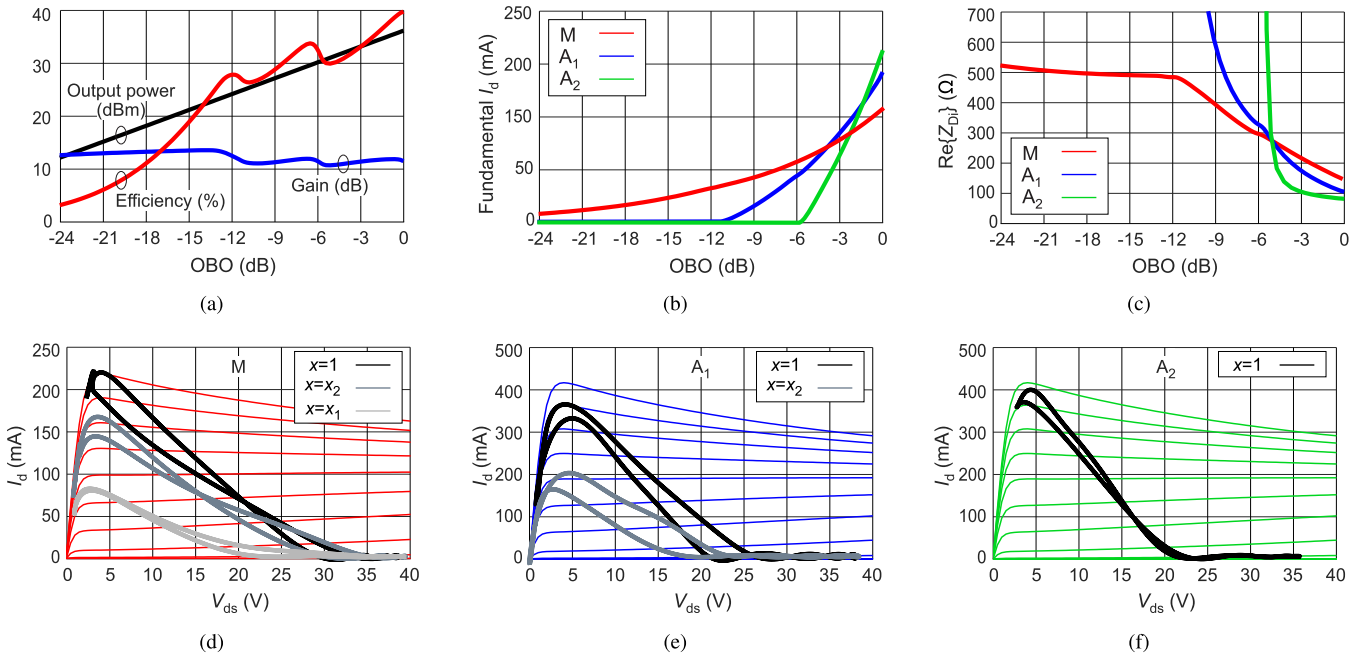

Fig. 11. Simulation results of the two-stage DPA3W with lossless IMNs and ISMNs and lossy output combiner, with three separate RF inputs optimized at 28 GHz. (a) Output power, efficiency, and gain; (b) fundamental intrinsic drain currents; and (c) intrinsic drain resistance versus OBO, and dynamic load lines of (d) M, (e) A_1, and (f) A_2 at the intrinsic drain terminal, at $x = x_1, x_2, 1$.

TABLE III
CIRCUIT PARAMETERS OF THE ISMNS AND IMNS

	ISMN						IMN		
	C_{is1} [pF]	C_{is2} [pF]	Z_{is1} [Ω]	θ_{is1} [°]	Z_{is2} [Ω]	θ_{is2} [°]	C_{i2} [pF]	Z_{i1} [Ω]	θ_{i1} [°]
M	0.4	0.4	66	71	42	48	0.9	70	10
A_1	0.5	0.2	62	45	42	33	3.7	65	10
A_2	0.4	0.3	53	57	40	39	3.6	70	10

TABLE IV
CIRCUIT PARAMETERS OF THE INPUT SPLITTER

Z_{b1} [Ω]	Z_{b2} [Ω]	Z_{b3} [Ω]	Z_{b4} [Ω]	Z_{b5} [Ω]	θ_{b1-5} [°]	R_{iso} [Ω]	Z_{del} [Ω]
98	66	21	85	87	90	147	50

the input impedance of the stabilized driver devices into 50 Ω. In both cases, a similar low-order filter topology (including the required dc feed and dc block components) is adopted for all branches, in order to limit the difference in phase rotation versus frequency and to trade off between compactness and bandwidth. The ISMN and IMN topologies, shown in Fig. 9, are optimized separately for each branch, due to the different bias conditions and periphery of the devices. The values of their circuit parameters are reported in Table III.

Once the combiner and MNs have been designed, the two-stage DPA3W is first simulated with three independent RF inputs whose relative magnitudes and phases are optimized at f_0, as shown in Fig. 10. The non-linear models of the transistors are used, and the gate bias voltage of each is tuned to ensure the proper turn-on. Despite having in theory as many degrees of freedom as transistors, a unique gate bias voltage is used for the driver and power transistors of the same branch (i.e., $V_{GdM} = V_{GM}$, $V_{GdA1} = V_{GA1}$, $V_{GdA2} = V_{GA2}$), which reduces the complexity and still allows to synthesize the required current profiles. The required splitting ratios ($P_{in,M}/P_{in} = 0.1$, $P_{in,A_1}/P_{in} = 0.22$, $P_{in,A_2}/P_{in} = 0.68$), and the fact that the linear gain of the Main amplifier chain is around 22 dB, allows to predict an overall gain around 12 dB for the whole two-stage DPA3W.

Fig. 11 reports the simulated performance of the two-stage DPA3W at 28 GHz, adopting the device non-linear models. The power gain is estimated assuming an ideal (lossless) input power splitting, for which $P_{in} = P_{in,M} + P_{in,A_1} + P_{in,A_2}$. Thanks to the optimized input driving, the obtained efficiency curve Fig. 11(a) and fundamental current profiles Fig. 11(b) are very close to those predicted by the theory. Indeed, the real part of the impedance Fig. 11(c) and the dynamic load lines Fig. 11(d)–(f) at the intrinsic drain planes of the three final devices confirm that the expected load modulation takes place. The gain of the two-stage DPA3W is around 12 dB in small signal and 10 dB at saturation, as expected, and its saturated output power is approximately 3.5 W. The efficiency peaks are around 30% at OBO, 35% at OBO_2, and 40% at saturation, respectively. These are compatible with the performance estimated for the selected devices and the combiner losses estimated in Fig. 8(d), which are higher in back-off and lower at saturation.

D. Predriver and Input Splitter

The DPA3W is completed by implementing a three-way analog splitter that feeds the branches with the required power and performs the signal alignment. Furthermore, since the gain

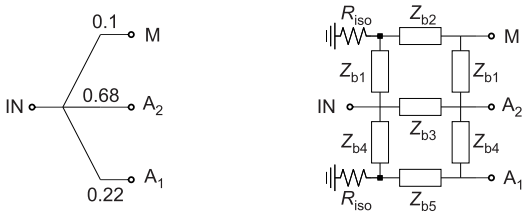

Fig. 12. Schematic of the three-way input splitter.

estimated for the two-stage DPA is of the order of 10 dB, a predriver stage is inserted in front of the power splitter.

Since the drivers are biased in different classes (M in class AB, A_1 in shallow class C, A_2 in deep class C), and it is likely that bias tuning will be required after fabrication to achieve the desired turn-on of A_1 and A_2, a non-isolated power splitter is avoided due to the high sensitivity to the drivers input impedance, which may not be accurately predicted by the foundry non-linear model. An isolated power splitter provides a safer alternative, at the expense of additional losses and larger area occupation.

A three-way isolating splitter could be implemented as a cascade of two two-way power splitters, or as a single-stage 1:3 splitter. The latter is chosen to minimize area occupation. A double branchline structure, shown in Fig. 12, can synthesize the desired splitting ratios with reasonable accuracy, while providing output ports isolation of at least 10 dB. Since a 90° phase shift is present between adjacent output ports, appropriate delay lines have to be inserted on each branch. The circuit parameters are summarized in Table IV, where all the splitter TLs are 90° at f_0, the three output ports are matched to 50 Ω, and the input port impedance is 10 Ω. The latter is convenient to simultaneously keep the TLs characteristic impedances within feasible values and ease the design of the OMN of the predriver device (4×75 μm), which is implemented with a stub-line topology. The branchline splitter is implemented in semi-lumped form, mainly to favor layout compactness, where the low-impedance TLs are replaced by their π equivalent networks, as done for the combiner and PMN. Finally, the IMN of the predriver is analogous to the IMNs of the A_1 and A_2 drivers, since they are based on the same active device.

IV. Fabrication and Experimental Results

The resulting three-stage DPA3W MMIC, shown in Fig. 13, has an area of 3.73×4.2 mm^2. It has been fabricated, mounted on a brass carrier with low-temperature solder paste, and dc and RF probed for the experimental characterization. The adopted dc probes are equipped with capacitors for low-frequency decoupling.

The DPA3W has been experimentally characterized in the nominal bias point $V_{DD} = 20$ V for all devices, $V_{Gpd} = V_{GdM} = V_{GM} = -1.8$ V, $V_{GdA1} = V_{GA1} = -2.2$ V, $V_{GdA2} = V_{GA2} = -2.6$ V, corresponding to an overall quiescent drain current $I_{D,tot} = 20$ mA.

A. Continuous Wave (CW) Measurements

The CW characterization has been performed with a pre-calibrated scalar setup. The input and output powers are measured in real-time with Keysight U8485A power meters. Fig. 14 reports the comparison of the CW simulated and measured performance of the DPA3W at the design frequency of 28 GHz. Fig. 14(a) PAE, Fig. 14(b) gain, and Fig. 14(c) total dc drain current (including predriver, drivers and final stages) curves plotted versus output power show a very good agreement between simulations and measurements, except for a difference of a few percentage points in terms of PAE around the turn-on point of the A_2 branch. To confirm the correct turn-on of A_1 and A_2 at 6 and 12 dB OBO, respectively, the individual dc drain current contributions of M, A_1, and A_2 (final stages only) are also reported in Fig. 14(c). Only simulated data are available in this case, since the layout of the combiner does not allow to separate such contributions. The overall agreement of the obtained results proves the effectiveness of the presented design strategy.

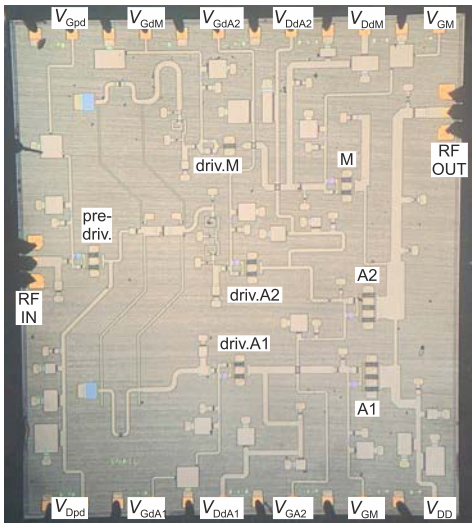

Fig. 13. Microscope photograph of the DPA3W (3.73×4.2 mm^2).

Furthermore, the DPA3W maintains a relatively flat response over a 1 GHz frequency band, from 28 to 29 GHz, as shown in Fig. 15. The saturated output power is between 34 and 34.3 dBm, with associated PAE and gain in excess of 20% and around 10 dB. The PAE is in the range 13%–16% both at 6 and 12 dB OBO.

The performance of the DPA3W is summarized and compared to the State Of the Art (SOA) in Table V. The results prove to be competitive over a 1 GHz band, especially in terms of efficiency at deep back-off, although not outperforming two-way DPAs [26], [27] in terms of efficiency at saturation and at 6 dB OBO. Furthermore, the PAE is strongly affected by the complexity in terms of presence/absence of driver stages, and thus by the gain. Single-stage DPAs [28] can achieve a remarkable efficiency even at these frequencies, but inevitably feature a very limited gain.

All in all, the theoretical advantages of a DPA3W at 5G FR2 frequencies may be hindered by the complexity of the architecture, especially to recover the inherently low gain. Therefore, future work will focus on the further simplification of the architecture and minimization of the losses.

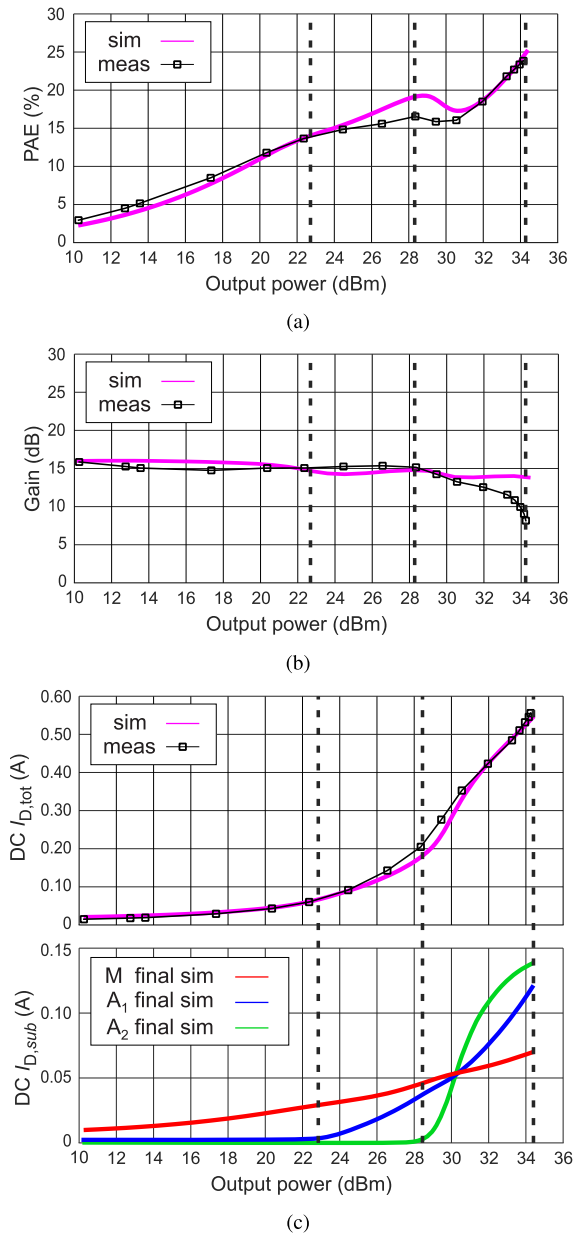

Fig. 14. Comparison of simulated (solid) and measured (black, symbols) CW performance of the DPA3W at 28 GHz (a) PAE, (b) gain, and (c) total dc drain current (top), compared to the simulated individual contributions of the final stages (bottom). The vertical dashed lines highlight the saturation and the 12 and 6 dB OBO turn on points of the auxiliaries.

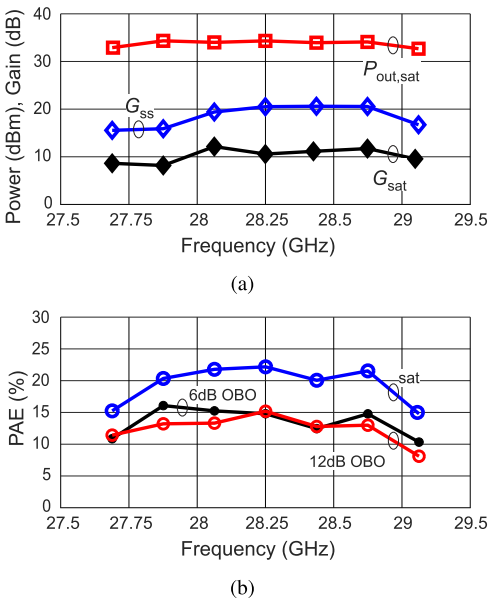

Fig. 15. Measured CW performance of the DPA3W from 27.5 to 29.25 GHz (a) saturated output power, saturated and small signal gain and (b) PAE at saturation, 6 dB OBO, and 12 dB OBO.

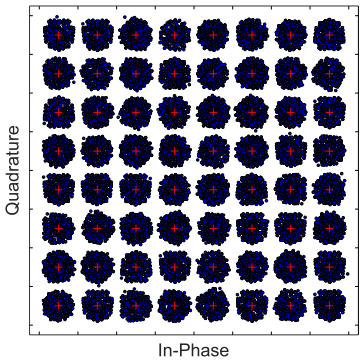

Fig. 16. Measured received constellation at 15 dBm average output power, with associated EVM $<$ 5% and ACPR $<$ -32 dBc.

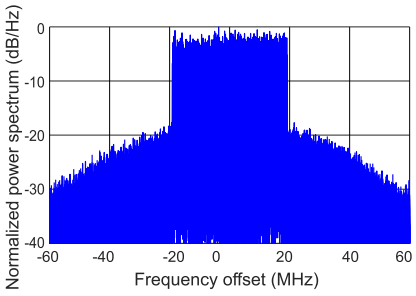

Fig. 17. Normalized output power spectrum at 25 dBm average output power, with associated PAE of 14% and ACPR $<$ -20 dBc.

B. Modulated Signal Measurements

The DPA3W has then been characterized at 28 GHz under modulated signals excitation to assess its inherent linearity, i.e., without the assistance of digital predistortion. The adopted signal is a 5G NR downlink compliant 64-QAM with 40 MHz instantaneous bandwidth, compatible with the limitations of the available setup. The corresponding PAPR of the signal is 10 dB.

The adopted measurement setup includes a Keysight E8267D PSG for the signal generation and up-conversion and a Keysight N9021B MXA as receiver. The baseline EVM and ACPR measured using an on-wafer thru are $<$1% and <-48 dBc, respectively.

The linearity requirements of the 3GPP for 64-QAM 5G NR signals [29] (EVM $<$ 8% and ACPR $<$ -28 dBc) are satisfied until an average output power of 17 dBm. At an average output power of 15 dBm, the DPA3W achieves EVM $<$ 5% and ACPR $<$ -32 dBc with associated PAE of 8%.

TABLE V
COMPARISON BETWEEN SOA *Ka*-BAND DPAS

Technology	Frequency band (GHz)	$P_{out,sat}$ (dBm)	PAE_{sat} (%)	$PAE_{6\,dB\,obo}$ (%)	$PAE_{9\,dB\,obo}$ (%)	$PAE_{12\,dB\,obo}$ (%)	Gain ss (sat) (dB)	Ref
45 nm CMOS SOI	28	22.4	30*	28	20*	15*	10* (5*)	[26]
28 nm CMOS	26	18.7	32*	15*	9*	5*	16* (12.5*)	[30]
28 nm CMOS	27	18.8	30	22	15*	10*	16.5 (10*)	[31]
28 nm CMOS	36	22.6	25*	24.2	12*	8*	18 (8*)	[21]
150 nm GaAs	27.25–29.75	27	37	25	15*	10*	18 (14*)	[32]
90 nm GaAs	28	30	38	30	18*	10*	17.4 (10*)	[33]
150 nm GaN-SiC	27–29	39	25	21	15	-	30 (-)	[34]
150 nm GaN-SiC	26–30	36.1	26.7	25	18*	12*	11* (7*)	[27]
150 nm GaN-SiC	24–28	34	23	14*	10*	-	18 (11)	[35]
150 nm GaN-SiC	29	30	40	28*	25*	20*	7 (6)	[28]
150 nm GaN-SiC	**28.5**	**34.2**	**22**	**15**	**14**	**15**	**20 (10)**	**This work**
	28–29	**34–34.3**	**20–22**	**13–16**	**12–15**	**13–15**	**15–20 (8–12)**	

* Value extrapolated from graphs.

The corresponding received constellation is shown in Fig. 16. At the highest measured average output power of 25 dBm, the DPA3W achieves ACPR < -20 dBc with associated PAE of 14%. Fig. 17 shows the corresponding measured output power spectrum.

V. CONCLUSION

This article has presented the theoretical design equations, a practical design strategy, and the implementation of a DPA3W. Based on the equations, design charts are drawn to explore the available design space. The proposed technique has been experimentally demonstrated by the design, fabrication, and characterization of a DPA3W adopting the WIN Semiconductors' 150 nm gate length GaN-SiC HEMT process. The DPA3W is optimized for 6 and 12 dB efficiency at 28 GHz, targeting 5G applications. The prototype achieves saturated output power in excess of 34 dBm and PAE of the order of 15% from 6 to 12 dB OBO, demonstrating competitive performance compared to the current SOA at similar frequencies. A very good agreement is found between simulations and measurements, thus proving the validity of the approach. A preliminary characterization with a 5G modulated signal has also been reported, demonstrating encouraging results in terms of efficiency-linearity trade-off.

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