Design and Validation of 100 nm GaN-On-Si Ka-Band LNA Based on Custom Noise and Small Signal Models

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Abstract: In this paper a GaN-on-Si MMIC Low-Noise Amplifier (LNA) working in the Ka-band is shown. The chosen technology for the design is a 100 nm gate length HEMT provided by OMMIC foundry. Both small-signal and noise models had been previously extracted by the means of an extensive measurement campaign, and were then employed in the design of the presented LNA. The amplifier presents an average noise figure of 2.4 dB, a 30 dB average gain value, and input/output matching higher than 10 dB in the whole 34–37.5 Ghz design band, while non-linear measurements testify a minimum output 1 dB compression point of 23 dBm in the specific 35–36.5 GHz target band. This shows the suitability of the chosen technology for low-noise applications.

Keywords: low-noise amplifier (LNA); gallium nitride (GaN); GaN/Si; GaN-on-Si; high linearity; HEMT; Ka-band

1. Introduction

Gallium arsenide (GaAs) is a material extremely suitable for high-frequency solid-state devices, components, and ICs (Integrated Circuits). The main peculiarities of GaAs-based devices are its high maximum frequency and low-noise behavior, even at frequencies over the Ka-Band [1,2]. As soon as GaAs grew in popularity for RF and microwave applications, silicon-based devices were rapidly replaced because of their much lower frequency limit and higher losses. The peculiar versatility of GaAs allowed the design and realization of different modules with remarkable performances [3–5], which could be assembled together, realizing more complex structures such as transmit-receive modules (TRMs). However, the main limitation of GaAs devices has always been the relatively low output power. In applications where high-power signals are exchanged, it is crucial to ensure the survivability of the MMIC (Monolithic Microwave Integrated Circuit) in any operative condition. Therefore, several functionalities needed protection circuits to ensure their correct operation. To provide examples, bulky ferrite circulators were used instead of SPDT (single-pole double-throw) MMIC switches, several HPAs (high-power amplifiers) have to be parallelized in order to satisfy a high power request, and limiter circuits have been frequently placed upstream of LNAs (low-noise amplifiers) to prevent their destruction [6]. This last indispensable solution represents a clear limit of the GaAs technology, thereby increasing the losses, overall dimensions, and noise figure (NF) of the whole structure. Moreover,

the mandatory need of this protection arrangements precludes the possibility of integrating several functionalities onto the same MMIC, as it generally happens in a single-chip front-end (SCFE). During the last decade we witnessed an exponential growth of gallium nitride (GaN) devices and MMIC production, with this technology becoming the favorite one in many RF and microwave applications. Indeed, GaN's main features, such as a wide bandgap, high velocity saturation, and a very high breakdown electric field make it a perfect technology for high-power requirements' satisfaction. The robustness of GaN devices allows them to tolerate much higher power signals, to the point of improving integrability and broadening the contexts of applications of RF MMIC circuits. GaAs devices maintain anyway an advantage not negligible at very high frequencies, especially regarding the noise behavior [7].

Since GaN HEMTs need other material as substrates, silicon carbide (SiC) has been adopted as the preferred material to the growth of GaN devices, and its performance have been widely shown in literature both for devices [8,9] and designed MMICs [10]. However, SiC wafers' production is very expensive, given the current difficulty to realize wide diameter wafers, making GaN-on-SiC technologies not suitable to mass industrial production. Furthermore, major manufacturers reside outside the European Union. This represents a serious bottleneck for the growth of European companies, GaN being an enabling technology for crucial RF applications. This situation brought the scientific community to research different materials as substrates for the realization of GaN devices.

In recent years, silicon (Si) has been identified as a suitable alternative to SiC in this context. The development of GaN-on-Si devices could be crucial to obtaining a remarkable reduction in the manufacturing costs, as the production of Si wafers is much cheaper. Moreover, the maturity of Si technology would allow the realization of larger-diameter wafers, with respect to their SiC counterparts. Lastly, the development of GaN-on-Si devices could supply European companies with an enabling technology for space-borne and critical applications, circumventing the necessity to import SiC wafers from other countries. However, the reason why SiC is the preferred substrate material for GaN devices resides in its still superior performance: GaN-on-Si devices, indeed, show lower gain and noise behaviors. This is due to different issues, such as the higher Si losses, a lower Si thermal conductivity compared to the SiC one, and the bigger lattice mismatch GaN has with Si respect to SiC, which brings a higher density of impurities and vacancies in the crystalline structure of the devices [11,12].

Nowadays, GaN-on-Si technology's evolution allows to obtain performances comparable to GaN-on-SiC devices, as the gap is not such as to discourage its adoption anymore, and robust designed MMICs results have been already presented in literature [13]. For this reason, the EU H2020 project "MiGaNSOS" has been set up, aiming mainly to the qualification of a GaN-on-Si technology, namely, the OMMIC D01GH, which could be employed at industrial level on a wide scale. With this aim, both a custom small-signal and noise model have been extracted and validated, and subquently a LNA has been designed. Presented results shall prove the suitability of this technology to the satisfaction of low-noise and high-power applications requirements, as also shown in a similar work by only simulated performance obtained by the means of a design kit provided by foundry [14].

2. Chosen Technology

2.1. Description

OMMIC's D01GH technology consists of an GaN/AlGaN HEMT epitaxially grown on a high resistivity (5 kΩ/cm), 100 μm thick silicon substrate. Channel length is equal to 100 nm, and its main features are reported in Table 1. As we can notice, the technology shows a satisfying maximum usable frequency of 160 GHz with a 1.5 dB NF at 40 GHz. The remarkable performance in terms of power density is confirmed by the 3.3 W/mm RF output power.

Table 1. D01GH's main features.

Parameter	Unit	Value
Gate Length	nm	100
Substrate Thickness	μm	100
f_T	GHz	110
f_{MAX}	GHz	160
RF Power Density	W/mm	3.3
Transconductance	mS/mm	800
Noise Figure @ 40GHz	dB	1.5
I_{Dss} Max	A/mm	1.7
Breakdown V_{GD}	V	36
V_{DD} for best noise	V	3 to 7
V_{DD} for power	V	12 to 13

The asymmetrical positioning and the mushroom shape of the gate contact was studied to raise the cutoff frequency of the devices, lowering the access resistances. Figure 1 shows a cross-section of the device.
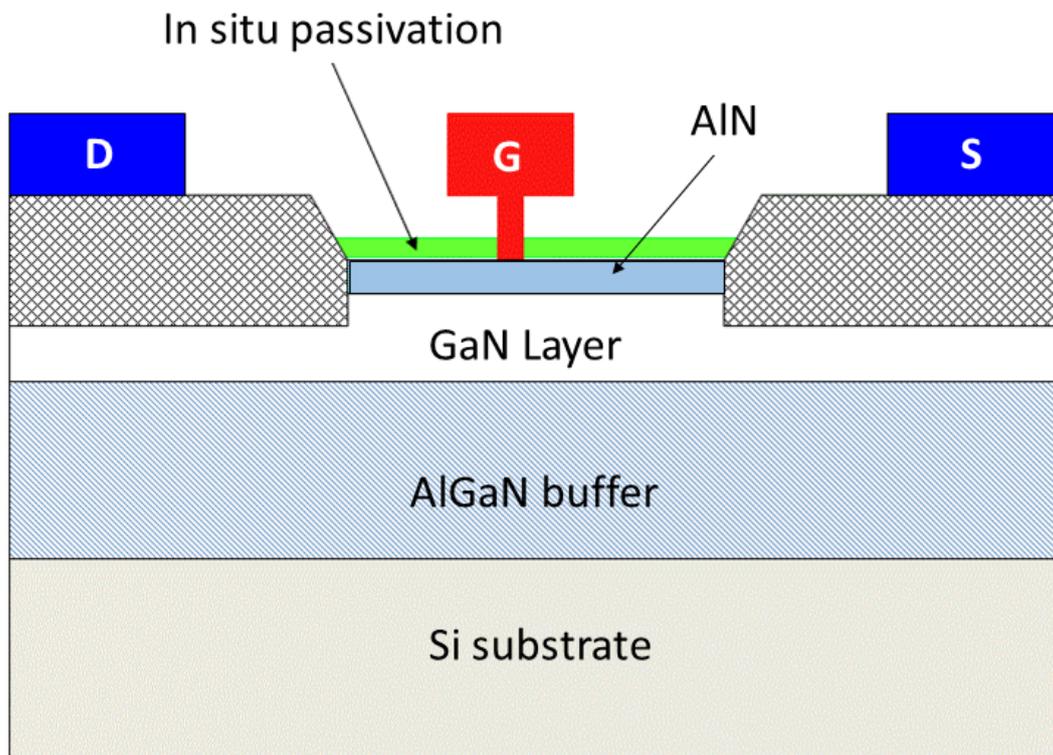
Figure 1. D01GH device's cross section.

The D01GH process also includes several passive components, such as two MIM capacitors to realize different capacity ranges (50 and 400 pF/mm^2), low and high precision resistors (40 and 400 Ω/square), inductors, transmission lines, via-holes, and all interconnecting components useful for a RF design. Models of passive components come in a design kit provided by OMMIC foundry. Figure 2 presents a cross-section of the whole D01GH process.
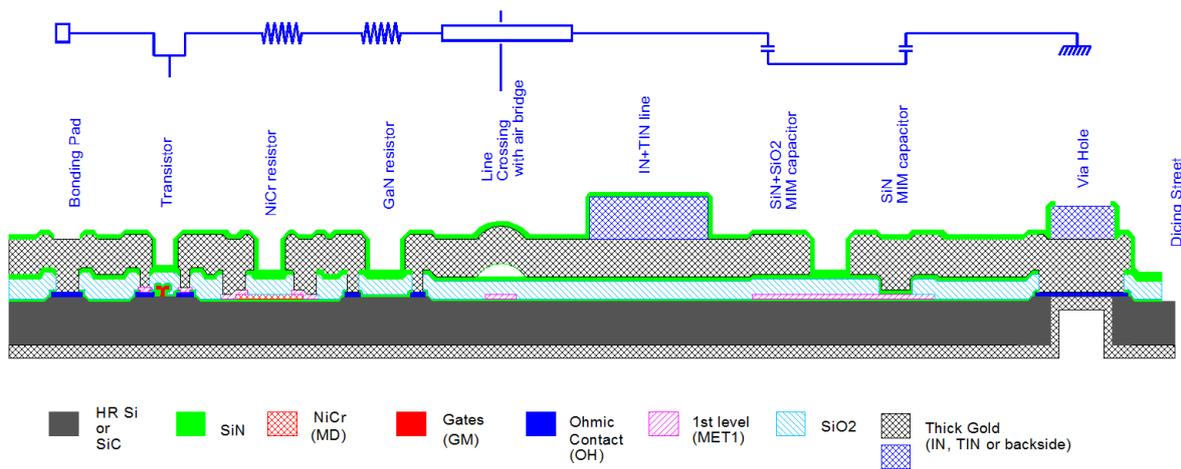
Figure 2. D01GH process cross section.

2.2. Modelling

One of MiGaNSOS project objectives is to model and validate D01GH devices in terms of small signal and noise behavior. Model extraction has been conducted through a measurement campaign carried out on a significant number of devices. In particular, families of devices with 2, 4, 6, and 8 gate fingers 35, 50, 70, and 100 µm wide have been measured. A preliminary DC screening has been conducted in order to identify a subset of devices statistically significant to obtain the most accurate extractable model.

Narrowed down the initial subset of devices, small signal measurements were carried out on the remaining transistors sweeping the V_{DS} from 0 to 12 V and the V_{GS} from -2 to -0.75 V, by making use of a LRRM calibration. Starting from the measurements taken in microstrip configuration, the via holes connected to the sources of the devices were carefully de-embedded by means of electromagnetic (EM) simulations performed in the Sonnet environment, taking account of an eventual coupling between the two vias, too. After choosing the equivalent circuit topology reported in Figure 3, an optimization algorithm was used to interpolate a small signal model scalable with gate width, fixing the number of fingers. This choice was preliminarily made in order to enhance model robustness to device non-uniformities and measurement errors. The model was then validated with a brief comparison of the measurements.
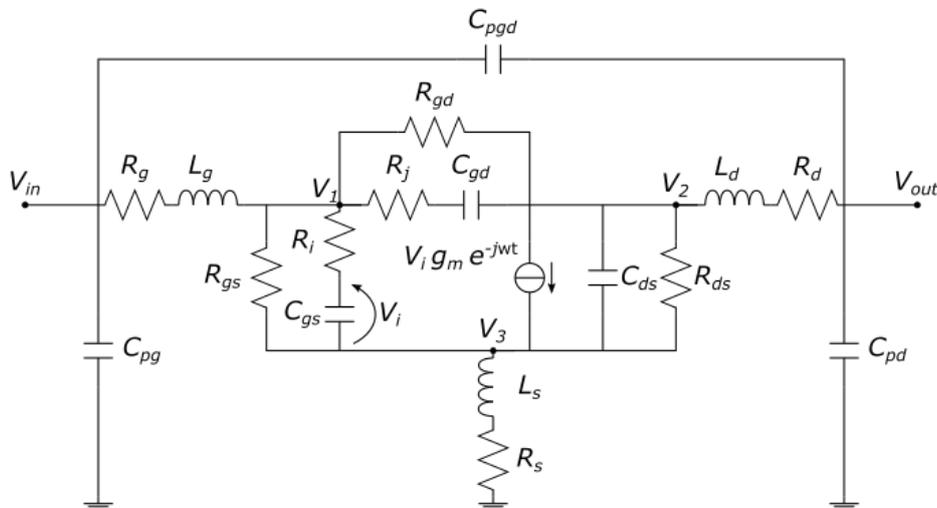

Figure 3. Equivalent circuit chosen for small signal model extraction.

The noise behavior of the D01GH technology was subsequently extracted in the DC-40 GHz frequency range through the common noise-temperature model, with two equivalent thermal noise sources assigned to gate and drain terminals, respectively, as in [15]. Those temperatures were extracted through noise factor (F) measurements performed on a well-matched input termination. This method allows the use of a much simpler measurement bench and easier post-processing, with a strongly reduced total number of measurements for the noise parameters' determination. The noise measurements were conducted on families of devices with 2, 4, and 6 gate fingers 50, 70, and 100 μm wide. V_{DS} was fixed to 2.5, 5, and 7.5 V, while V_{GS} ranged from -1.5 V to -0.75 V with a step of 0.25 V, accurately avoiding the drain and gate voltage combinations in which power dissipation limits would have been reached. As Figure 4 shows, the extracted model was validated with a brief comparison with the noise measurements carried out at the beginning, confirming the accuracy and the scalability of the model on every family of devices. The measured average NF behavior results were slightly higher than the model prediction. This is a direct consequence of deciding to extract a model not suited to the single geometry, but to whole families.
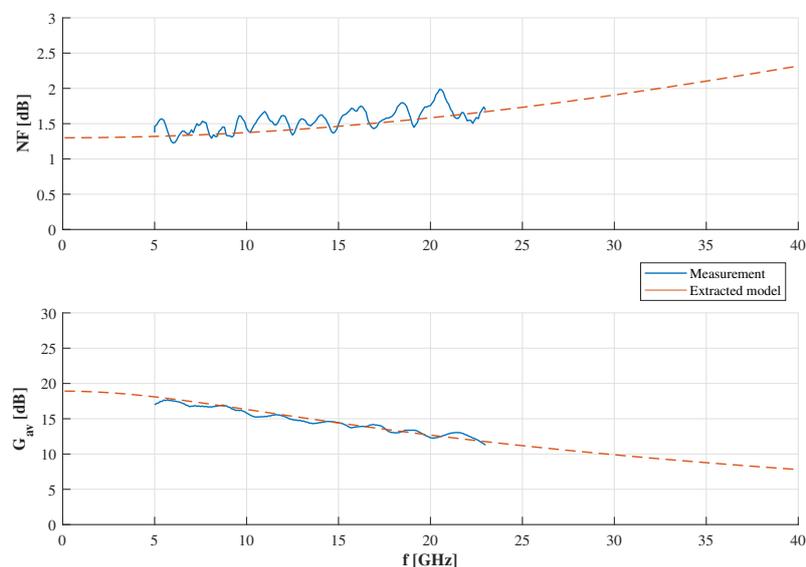

Figure 4. Noise figure (NF) and associated gain of a 2 × 50 μm device at V_{DS} = 5 V, V_{GS} = -1.25 V, Id = 31 mA: measurements versus simulations.

3. Test Vehicle Design

As a following step, a LNA was chosen to be designed employing the ad-hoc extracted small signal and noise models, in order to validate their accuracy, to test the D01GH technology's suitability to a low-noise modules' design, and to place it in the state-of-the-art framework. Design specifications are summarized in Table 2.

Table 2. Designed low-noise amplifier (LNA) specifications.

Parameter	Unit	Value
Frequency	GHz	34 to 37.5
Linear Gain	dB	≥30
Noise Figure	dB	≤2.5
I/O Return Loss	dB	≥10
Output 1dBcp	dBm	≥20

The 34–37.5 GHz range was chosen to be the design band, but the specifications had to be satisfied more specifically in the 35–36.5 GHz target band. Due to the high gain request, especially considering the Ka-band design band, a multi-stage approach was adopted. To conjugate the high-gain and low-noise requests, a device characterized by four gate fingers each wide 35 μm was chosen to design all the stages. In particular, Figure 5 shows the minimum noise figure (NFmin) and the associated gain of the selected geometry predicted by the extracted extracted models for V_{DS} = 5 V, V_{GS} = −1.5 V. At 35 GHz, models predict a 1.85 dB NFmin and a 9 dB associate gain.

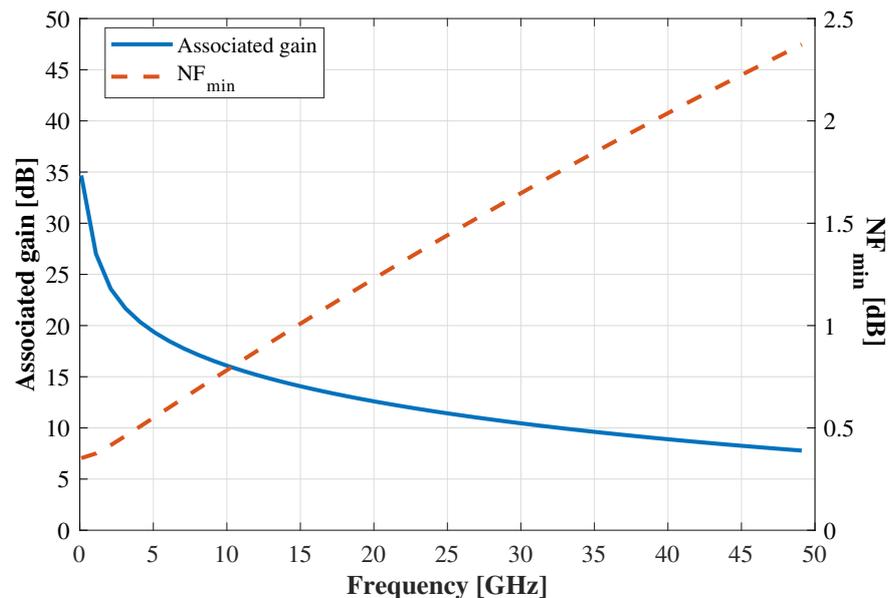**Figure 5.** Simulated associated gain and minimum noise figure (NFmin) of a 4 ×35 μm device predicted by the small signal extracted model at V_{DS} = 5 V, V_{GS} = −1.5 V. At 35 GHz, values are 9 dB and 1.85 dB, respectively.

A four-stage topology was selected, in order to compensate the inevitable network losses and to be sure to satisfy the high gain request. A double polarization scheme was chosen, with the aim of having a complete bias independence for gate and drain of every device involved. Furthermore, an inductive series-feedback was adopted to the source of every stage device, in order to ease the unavoidable trade-off between gain, noise, and matching, and to improve single stage stability, as well. As it is well known, the Friis formula is the major rule to keep in mind throughout the whole design of a LNA. It demonstrates how in a cascade of several amplifying stages, it is the first one to give the main contribution to the NF of the whole circuit, since the noise added by the following stages is mitigated by the gain of the previous ones. This requires a careful design of the first stage and of its input matching network (IMN) in particular, which should add the least amount of losses, guaranteeing a satisfying matching level with the source and showing the optimum noise termination to the input section of the device, in order to minimize its noise contribution. Furthermore, a suitable bias for low noise was chosen for first and second stage, while the following stages were biased so as to raise the gain of the cascade, as shown in Table 3.

Table 3. The LNA stages' biases and power consumption.

	Unit	1st stg	2nd stg	3rd stg	4th stg
Periphery	μm	4 × 35	4 × 35	4 × 35	4 × 35
$\mathbf{V_{DD}}$	V	5	7.5	7.5	7.5
$\mathbf{I_D}$	mA	16	25	69	69
$\mathbf{P_{DC}}$	W	0.08	0.18	0.52	0.52

In LNAs design, the conjugation of low-noise, high-gain, and good I/O matching requirements might be extremely tedious [16]. In particular, IMN is crucial for both low-noise and input matching of the amplifier, so it is mandatory to search design methods that allow the designer to obtain the best available trade-off between this figures of interest, while assuring the satisfaction of all performance specifications. As a design choice, the optimum noise measure termination was shown to the input section of all devices, in order to minimize the NF of the cascade. More specifically, a deterministic design approach, namely, the "constant mismatch circles" method, was adopted for first and second stage preliminary design [17]. Conceiving a mismatch at the interstage sections, and imposing the optimum noise measure load at the input section of all devices, by tuning the source-inductor values, we can obtain a satisfying level of input and output matching while still ensuring the lowest achievable noise of the whole amplifier. This method was tailored for two stage LNAs at first, but could be extended to more complex structures.

After applying the described method to identify the terminations to show at every section of the device, matching networks were designed, starting with ideal components while trying to use the least number of them. All networks were designed through a C-series, L-shunt topology, in order to employ a DC-block on the RF path and a high-impedance line at the operating frequency towards the DC supply. Frequency limits of the inductor circuit model provided by the foundry could not allow us to use this particular component for this specific design. For this reason, inductors were replaced by narrow transmission lines exhibiting high characteristic impedance for both the matching networks and the source feedback inductances.

Matching networks were therefore designed by the means of a hybrid lumped-distributed topology, which uses MIM capacitors, transmission lines, and short-circuited stubs. Wherever it was needed, a series of two bigger capacitors was used to realize small value capacitances, so as to minimize harmful effects of eventual process variations. At first, topologies of matching networks using short-circuited and open-circuited stubs were considered. A brief comparison showed how in the operative frequency range short-circuited stubs were much more convenient in terms of dimensions and introduced losses. Moreover, this kind of stub allowed us to correctly bias the devices without introducing complex structures to feed the circuit, which was something that would not be directly possible with open-circuited stubs. ISMNs (inter-stage matching networks) have been designed as a three-element structure with two short-circuited stubs separated by a capacitor, in order to correctly decouple the DC paths of gate and drain of two adjacent stages. Ohmic losses were not added on the RF paths so as to not degrading the noise performance of the LNA. Given the relatively high current values flowing through the DC drain paths, resistors were not placed there either, since they would have reached excessive width dimensions. However, resistors were placed in the DC gate paths to improve single stage stability and dampen eventual instability loops. Finally, decoupling networks were designed. A topology was built on a couple of high value shunt capacitors, and a very small series resistance was chosen. This structure was adopted to dampen the quality factor of the network, making the load synthesized not purely reactive in case of resonances. Component sizing was conducted verifying the low sensibility of the reflection coefficient downstream of the decoupling network's varying DC-feed load. An absolutely steady behavior was obtained for frequencies above 800 MHz, with no significant effect below this value. Figure 6 shows a simplified schematic of the designed MMIC.

Subsequently to circuit design finalization, ensuring the fulfillment of all requests, electromagnetic (EM) simulations were conducted to validate design reliability. Despite the apparent simplicity of matching networks, EM simulations showed strong performance shifts. In particular, the input matching network strongly contributed to a variation of the circuit behavior. This needed a heavy EM optimization by the means of some crucial components tuning for every matching network, in order to match the performance of pre- and post-EM design.
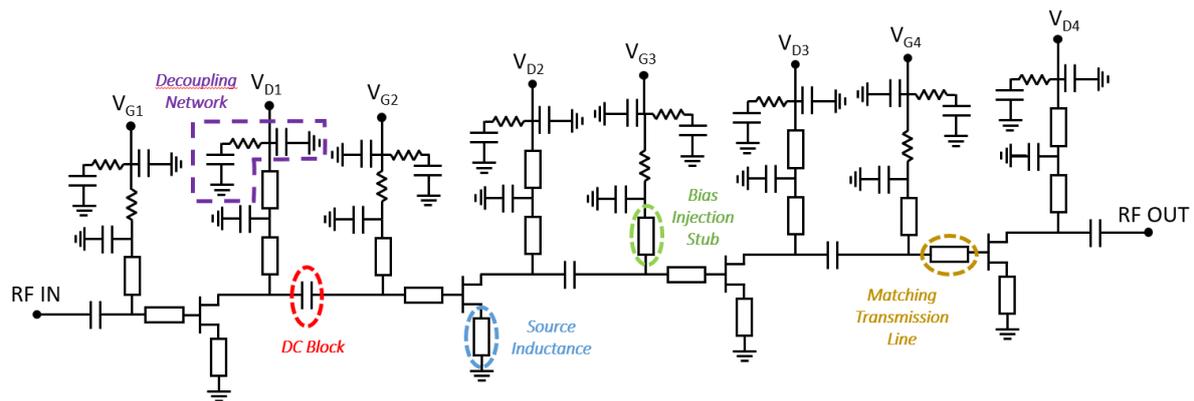
Figure 6. Simplified circuit scheme of the designed LNA.

4. Layout and Performance

Figure 7 shows LNA's post-EM tuning layout, and a microphotograph of the realized MMIC. From left to right, we can easily recognize the RF input port, the four stages with their matching and DC networks, and the RF output port. DC pads for drain and gate bias are located on the upper and lower side of the MMIC, respectively. Every stage has its own couple of pads for gate and drain bias, even if several devices share the same supply voltage, in order to avoid potential instability loops and to obtain a higher degree of freedom during a measurement phase. The MMIC has overall dimensions of 3.6×2 mm^2. In the following figures, the simulated performance of the amplifier after the EM tuning of several networks is shown.
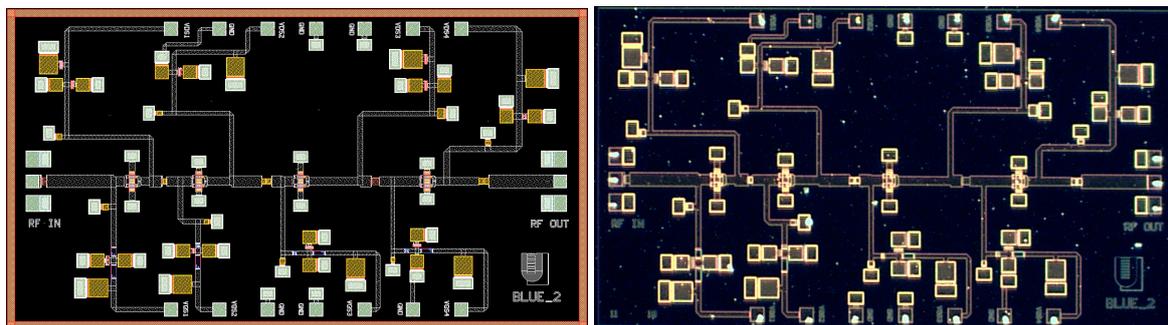

Figure 7. Layout and microphotograph of the designed LNA MMIC. Size is 3.6×2 mm^2.

Figure 8 depicts the gain and NF of the LNA. The first reaches an average value of 30 dB in the design band. NF shows its minimum value in the design band, which stands at 2.3 dB. This confirms the suitability to low-noise applications for this peculiar technology. Figure 9 reports input and output matching level of the amplifier. They both reach a value higher than 10dB in the design band, with S_{22} showing a wider band behavior, since IMN has to guarantee impedance matching for return loss and low noise at the same time. Some stability simulations up to 110 GHz were carried out, checking the behavior of µ factor, in order to confirm the unconditional stability of the whole amplifier. For non-linear simulations, models provided by OMMIC foundry through a pdk were used. Figure 10 shows the output power level for fundamental and third harmonics versus the available source power fixed at 35.75 GHz. The output 1 dB compression point (O1dBcp) is expected to be around the 24 dBm level, which corresponds to a −7 dBm input power value. By tracing the linear extension of these curves, output third-order intercept point (OIP3) can be evaluated: it lies around the 32 dBm level.
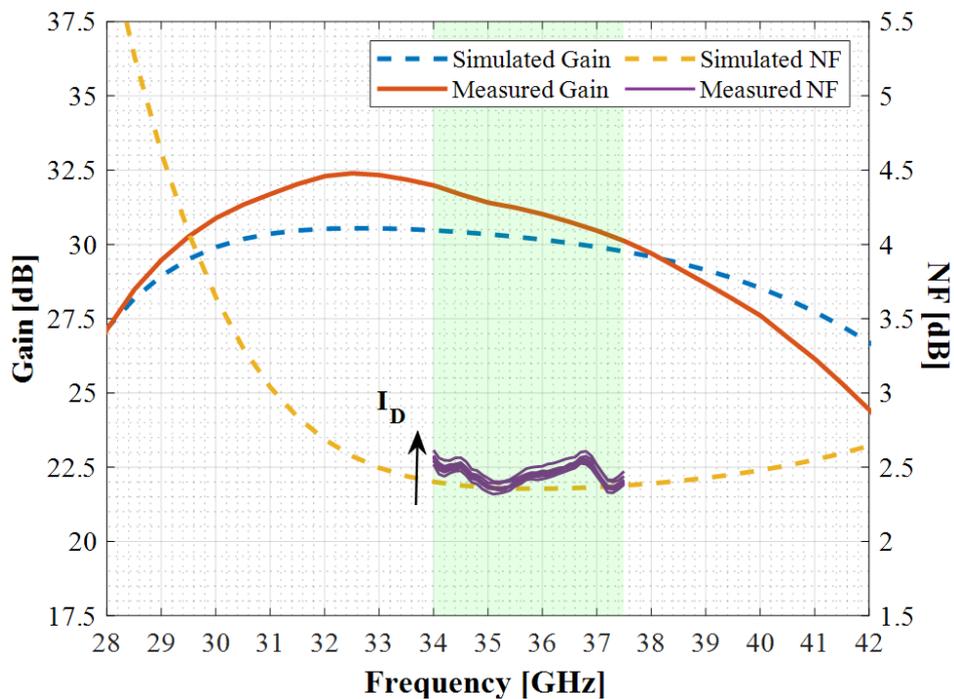
Figure 8. Gain and NF of the designed LNA. Dashed lines represent simulations, while continuous lines depict measurements. The narrowband purple traces represent the NFs of two different LNA cells measured at different I_D values.
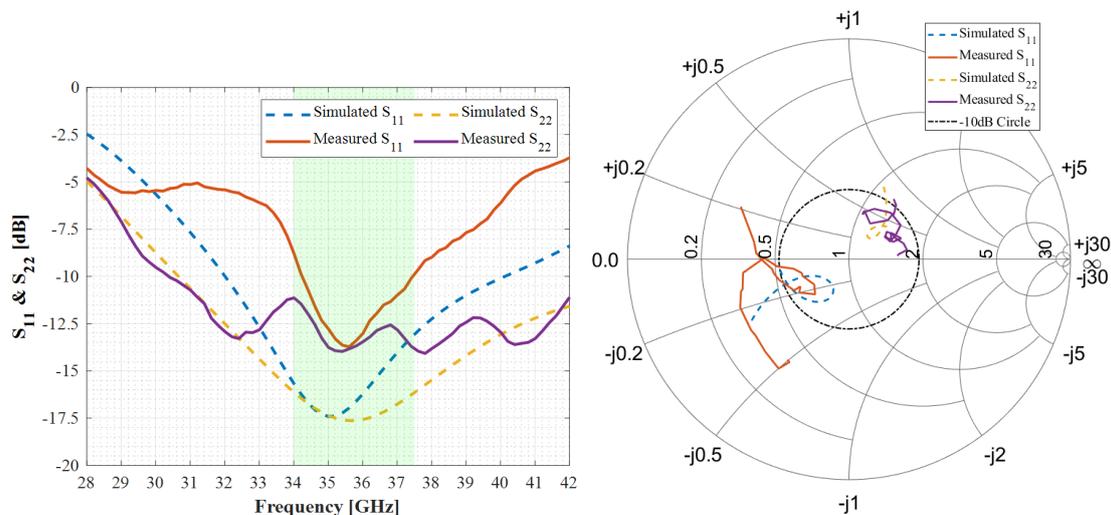

Figure 9. S_{11} and S_{22} of the designed LNA in absolute value and Smith chart. Dashed lines represent simulations, while continuous lines depict measurements. Traces in the Smith chart graph represent the LNA behavior between 30 and 40 GHz.

Further nonlinear simulations were implemented to test the expected power handling of the selected technology. Table 4 reports the instant currents and voltages values that bring the device to destruction as suggested by OMMIC foundry. The graphs given in Figure 10 show the istantaneous values of V_{GS}, V_{DS}, V_{GD}, and I_G for a value of RF available source power between -10 dBm and -3 dBm, which corresponds to an output power value of 24 dBm. As we can see, I_{G4} represents the strongest limit, exceeding the value of 80 mA for -3 dBm available source power. Given the high gain value, the fourth stage represents a strong limit in this context: the stages up to the third one would bear a much higher value of RF available power before reaching the limits reported by the technology manual. However, this is just a primarily evaluation. Additional insight shall be provided

by power-robustness measurements. These results shall confirm the suitability of this technology and design for high-linearity and power-handling contexts.
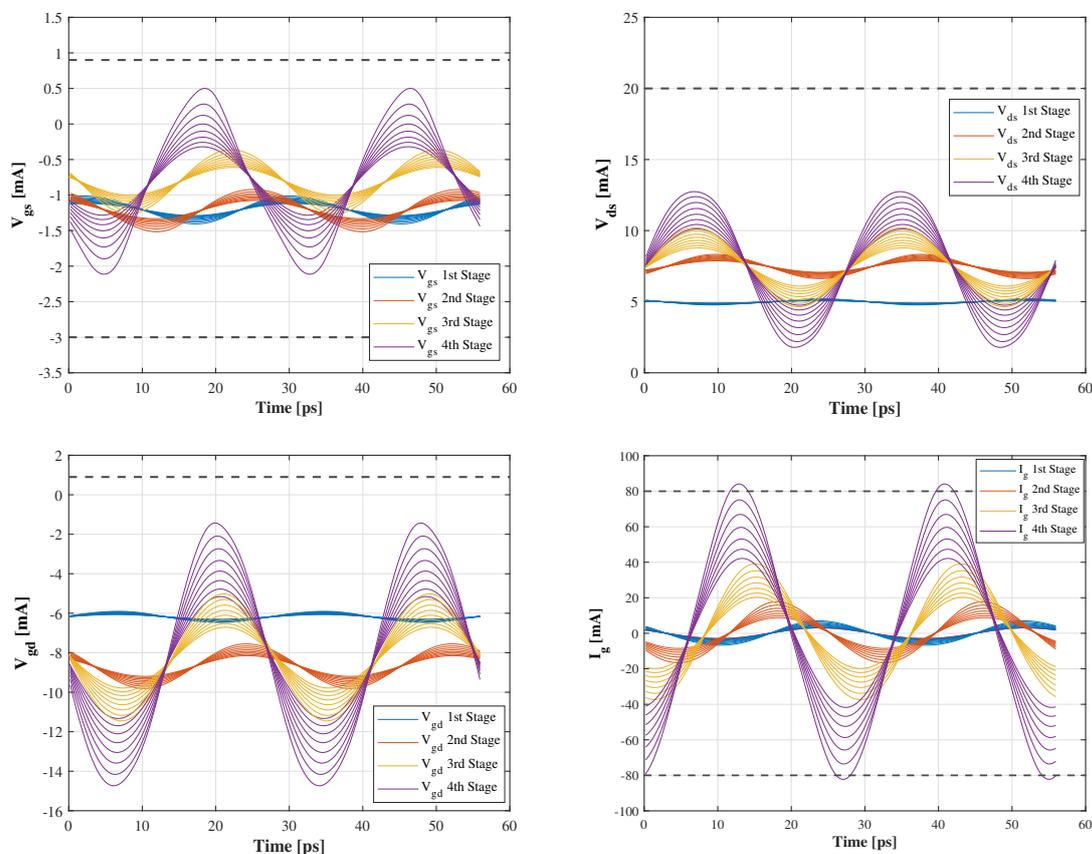

Figure 10. Simulated instant values of V_{GS}, V_{DS}, V_{GD}, and I_G versus time for every stage of designed LNA corresponding to an available source power between −10 and −3 dBm. Black dashed lines represent the limits reported in Table 4.

Table 4. D01GH breakdown currents and voltages.

Parameter	Unit	Value
V_{gd}	V	−30 to +0.9
V_{gs}	V	−3 to +0.9
V_{ds}	V	−20 to +20
I_g	DC mA/finger	2
I_g	DC + RF mA/finger	20

S-parameter measurements on the designed LNA were taken with a HP 8510 VNA, using a 128 samples average. A 10 dB attenuator was used to carry a −25 dBm available power level to the MMIC. To draw a direct comparison, Figure 8 contains the measured gain and noise of a statistically significant LNA cell as well. We can observe the S_{21} measured behavior, which was slightly higher than the simulations, standing at 31 dB with a stronger slope. Still in Figure 8, a narrowband (34–37.5 GHz) NF behavior is depicted for two different tested cells, also varying the drain bias between 4 and 7.5 V for every stage. We obtained a satisfying agreement with expectations, collecting a 2.4 dB average measured value in the whole operative band. The discrepancies between measured and simulated NF can be attributed almost exclusively to measurement uncertainty, which cannot be neglected in this frequency range, and to a finite matching level of the measurement test-bench, which affects the source termination of the first stage. With regard to the S_{21}, differences can be partially assigned to a higher

transconductance, featuring the realized transistors compared to models, and partially to differences in measured and simulated S_{22}.

In Figure 9 we can observe the measured S parameters of a significant cell. Matching levels are different than those predicted, but the graph shows how the measured parameters present their minimum value in the expected frequency band, confirming the validity of extracted small signal model. Still in Figure 9, we can see the S_{11} and S_{22} behavior on Smith chart. In particular, as to the S_{11}, only minor magnitude and phase deviations can be observed. Some shape discrepancies can be noticed in the S_{22}: on the Smith chart, the measurement trace is featured by two loops, as opposed to simulations, which present just a single curl. This additional loop translates in the multiple peaks on the magnitude of the measured S_{22}. This unexpected behavior can be ascribed both to undesired coupling between adjacent matching networks and to the interaction between external biasing circuit and internal decoupling networks, producing unexpected resonances. Some minor deviations can be also ascribed to the adopted calibration technique, a standard SOLT on a commercial Al_2O_3 substrate which cannot correctly take into account the effect of coplanar-microstrip transition at the input and output of the LNA.

Several power measurements were carried out in the specific 35–36.5 GHz target band, in order to test the remarkable features in terms of linearity and power handling of D01GH technology. As Figure 11 shows, we obtained a measured O1dBcp of about 23–24 dBm, a value well-matching the one foreseen by simulations.
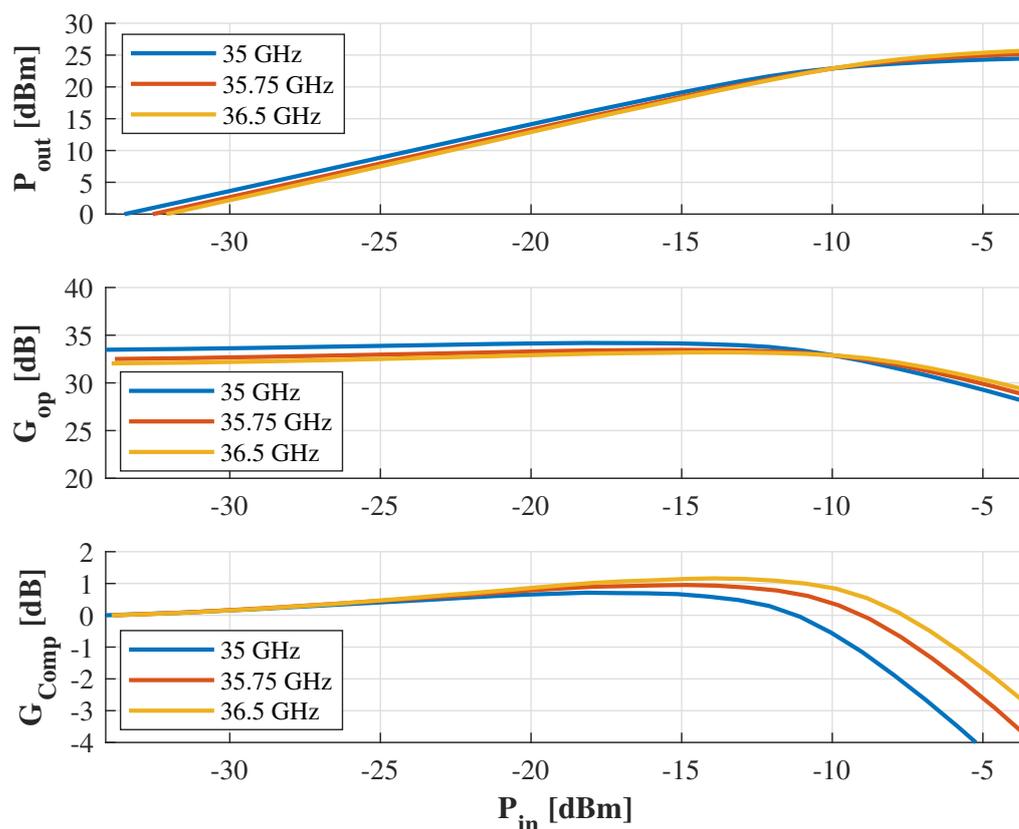

Figure 11. Measured output power, operative gain, and gain compression of a tested LNA cell at the bottom, middle, and top operative bands.

Table 5 summarizes the performance of the presented LNA and draws a brief comparison with others published state-of-the-art works. The present work shows a noteworthy level of gain, especially considering the relatively high working frequency. Its NF value is remarkable, especially considering the chosen technology and the relatively high working frequency. It is worth noticing that the comparison is drawn mainly with GaN-on-SiC technologies, which should present a better overall performance. In addition to the comparable or better performance in term of NF, the present work presents the highest measured 1 dBcp, along with the best value of O1dBcp/P_{DC} efficiency. This confirms the noteworthy features of the D01GH technology and its robustness and suitability to low-noise, high-linear requirements.

Table 5. Performance comparison with published works.

Ka-Band GaN LNAs	Unit	[18]	[19]	[20]	[21]	[22]	This Work
Substrate		SiC	SiC	SiC	SiC	Si	Si
Gate Length	[nm]	150	150	150	40	150	100
Frequency	[GHz]	25 to 35	27.5 to 28.5	27 to 31	27 to 40	35.5	34 to 37.5
Avg Gain	[dB]	$\geq$20	18	$\leq$20	$\leq$27	17	31
Avg NF	[dB]	$\geq$3	4	$\leq$3.9	$\leq$1.6	2.9	2.4
I/O Return Loss	[dB]	$\geq$10	$\geq$6.5	$\geq$7	$\geq$5	$\geq$9	$\geq$10
Output 1dBcp	[dBm]	-	$\geq$12.5	-	11	-	23
P_{DC}	[W]	0.36	0.2	-	0.082	0.3	1.3
O1dBcp/P_{DC}	[%]	-	8.9	-	15.3	-	19
Size	[mm^2]	2.6 $\times$ 0.8	3 $\times$ 2	3.4 $\times$ 1.2	3.1 $\times$ 1.12	-	3.6 $\times$ 2

5. Conclusions

In this contribution, a low-noise amplifier operating in the Ka-Band designed on a GaN-on-Si technology has been presented. The chosen technology, namely the OMMIC D01GH, was deeply studied, and both small signal and noise parameters models have been extracted and exploited for the circuit design. The MMIC presents an average gain of 31 dB in the whole design band, while showing an average NF of 2.4 dB. A good linearity was proven by the 1 dBcp value measured at 23 dBm, and we expect by simulations a high robustness with the I_g exceeding the foundry suggested limit only with -3 dBm available source power. The chosen technology shows more than satisfying performance and suitability to low-noise, high linearity, and power handling requirements, showing itself as a robust candidate for crucial space-borne applications.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

DC	Direct current
EM	Electromagnetic
GaAs	Gallium arsenide
GaN	Gallium nitride
HEMT	High electron mobility transistor
HPA	High power amplifier

IC	Integrated circuit
IMN	Input matching network
ISMN	Inter-stage matching network
LNA	Low-noise amplifier
LRRM	Line reflect reflect match
MIM	Metal-insulator-metal
MMIC	Microwave monolithic integrated circuit
NF	Noise figure
NFmin	Minimum noise figure
OIP3	Output third harmonic intercept point
O1 dBcp	Output 1 dB compression point
RF	RadioFrequency
SCFE	Single-chip front-end
Si	Silicon
SiC	Silicon carbide
SOLT	Short open line thru
SPDT	Single-pole double-throw
TRM	Transmit-receive module
VNA	Vector Network analyzer

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