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S-Band Class-C-F Power Amplifier with 2nd Harmonic Control at the Input

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Received: 2 December 2019; Accepted: 26 December 2019; Published: 29 December 2019



Abstract: Power amplifiers (PAs) are the most power-consuming devices in a transmitter. Their performance in efficiency is crucial to the efficiency of the whole system. Therefore, the issue of high efficiency PA has remained hot over the years. This paper presents an approach to design an S-band single stage class-F PA biased in class-C condition. Through the manipulation of the 2nd harmonic at the input, shaping the voltage waveform at the gate node, a class-F PA with proper output matching network (OMN) is realized. The proposed class-C-F PA achieved 60% drain efficiency (DE) and 36.3 dBm of output power around the 3 dB compression point. The methodology of taking the input non-linearity into consideration is also presented. Its feasibility has been verified through both the design and measurements.

Keywords: power amplifier; class-C; class-F; gate harmonic control

1. Introduction

The topic of high efficiency power amplifiers (PAs) will persist as long as the communication industry flourishes. As the most power-consuming devices in a transmitter, PAs generate the most heat. Therefore, improvements in efficiency of PAs not only promote overall system efficiency but also relieve issues of the cooling system.

A traditional way to achieve improvements in efficiency is biasing a device deeper from class-A. It reduces conductive angle, while sacrificing the gain (up to 6 dB for class-B biasing point and even more for class-C). However, taking the advantage of properly-phased harmonics, in shaping the voltage and current waveforms at the active device output, leads to the minimization of power waste. In other words, the efficiency will be improved. In fact, waveform-engineering has demonstrated its effectiveness, while simultaneously increasing the output power delivered at fundamental frequency [1–4]. Various classes of PAs have been developed according to this approach when designing the relevant amplifiers [5–7].

A classic class-F PA, for instance, utilizes the 3rd harmonic to shape the drain voltage waveform into a rectangular wave [2,5,8,9], thus improving the output power, the drain efficiency (DE) and the gain up to 15% (theoretically) higher than the one achievable with a sinusoidal output voltage (i.e., tuned load case). Similarly, the proper generation and control of 2nd or 2nd and 3rd harmonic impedances would further improve the PA performances with respect to a tuned load configuration [2]. Besides that, other types of continuous mode PAs make use of harmonics together with the complex fundamental load to increase the bandwidth features, meanwhile maintaining the DE, gain, and output power at higher levels [10–12].

Harmonic manipulation has been proven to increase the effectiveness in performance improvement for single stage design solutions by properly exploiting the intrinsic non-linearity of the active device itself. However, most of the designs were biased at a class-AB biasing point. When a transistor is pushed into a class-C biasing range, instead of showing improvement in efficiency, it decreases due to the wrong phase displacement of the harmonic at the drain node, becoming unsuitable for the realization of a class-F PA. However, since the active device typically acts as a voltage controlled current source, there is the possibility to manipulate its voltage harmonic at the input, in order to properly modify the amplitude and phase relationship between the current harmonics and the fundamental one at the drain node [2].

This paper presents the design and experimental verification of a class-F PA biased in class-C, thus defining a new class-C-F PA. The realization and measurement results show the effectiveness of the above quoted harmonic manipulation at the input port of the device. In fact, by adjusting the loading impedance of the 2nd harmonic at the input, it can be properly modified for the output current harmonic contents, thus realizing a class-C-F PA by properly phasing the relevant 3rd harmonic at the output. The designed class-C-F PA achieves a DE higher than 60%, while supplying an output power of 37 dBm over a frequency range from 2.2 GHz to 2.5 GHz in simulation. In the measurement, it achieved a DE of 59.7% and output power of 36.9 dBm at center frequency, well in agreement with simulations.

2. Theory of the Gate Harmonic Control

The key to realizing high efficiency PA is to increase the fundamental power delivered to the load, while decreasing both the dissipating power and those delivering to the load at the harmonic frequencies. Harmonic manipulated PAs, based on III-V technology, such as GaAs or GaN, are usually based on the assumption that the active device acts as a current source controlled by the input signal. In particular, referring to FET (Field-effect transistor) devices, the current at the intrinsic drain node is mainly controlled by the voltage signal at the gate node, while the output voltage can be eventually shaped with proper harmonic load conditions.

It implies that the performances of a harmonic tuned PA depend not only on the proper impedance provided by the output matching network (OMN) at the relevant frequencies, but also on the amplitude and phase relationship between the harmonics and the fundamental frequency of the drain current, which in turns depend on the voltage signal presented at the gate node. Therefore, the gate bias condition, the input signal, and the loading conditions at the input determine the output current waveform, and in turn, the idea is implementable to perform a suitable output voltage waveform, shaping it in order to improve device performances. For example, let us consider a 3rd harmonic tuned PA, also known as class-F PA. The drain voltage can be written as [2]:

$$v_{DS} = V_{DD} - V_1 \cdot [\cos(\theta) + k_3 \cdot \cos(3\theta)], \quad (1)$$

where V_{DD} is the biasing voltage, V_1 is the fundamental component, and $k_3 = V_3/V_1$ is the ratio of the 3rd harmonic component V_3 with respect to the fundamental one V_1 . According to the theory of harmonic tuned PA, the optimum condition for achieving high efficiency is proceeding with $k_3 = -1/6$, resulting in the theoretical improvement of 15%. It means that the 3rd harmonic voltage has to be out of phase with respect to the fundamental one. When the device is driven by sinusoidal input signal, such a condition implies that the device has to be biased in class-B (theoretically) or in class-AB (practically). In fact, referring to the current harmonic components, reported in Figure 1, only for conduction angle from π (e.g., class-B) to 2π (e.g., class-A), the 3rd harmonic current is out of phase with the fundamental one, which is suitable for the realization of a class-F PA. Thus, since the output voltage harmonics is related to the relevant current ones through the passive OMN, the phase condition on the former can be attained only if the same phase condition holds for the current harmonics.

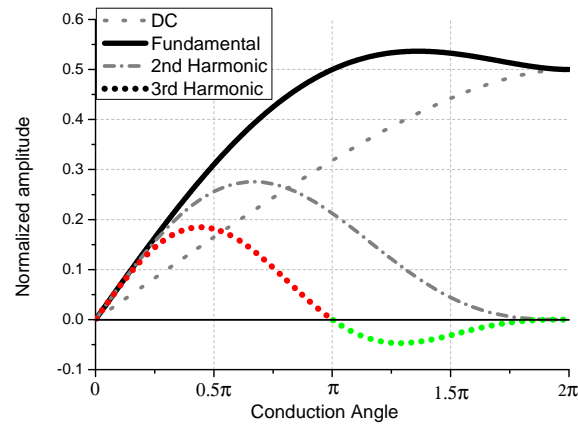


Figure 1. Intrinsic drain current harmonic stimulated by sinusoidal excitation. DC = Direct Current.

If the active device is biased in a class-C biasing range, the 3rd harmonic component of the intrinsic current is always in phase with the fundamental one; in other words, k_3 could hardly be negative in this condition. Such an improper phase relationship results in a detrimental effect to the performance of PA, which cannot be recovered by passive OMN, if a class-F output matching strategy alone is adopted.

However, things may be different if an alternative design strategy is adopted. One possible method is to form a rectangular current wave at the intrinsic current plane, in which case, the harmonics generated can be expressed as follows:

$$I_{r,n} = \begin{cases} I_{Max} \cdot \frac{\Phi}{2\pi} & n = 0 \\ \frac{2I_{Max}}{\pi} \frac{\sin(\frac{\Phi}{n})}{n} & n \geq 1, \end{cases} \quad (2)$$

where Φ is the conductive angle. As shown in Figure 2, with the different excitation, the biasing range where the 3rd harmonic is out of phase with respect to the fundamental one is from $\frac{2}{3}\pi$ to $\frac{4}{3}\pi$. Part of the conductive angle belongs to the class-C biasing range, which means that class-C-F PA is available under these conditions.

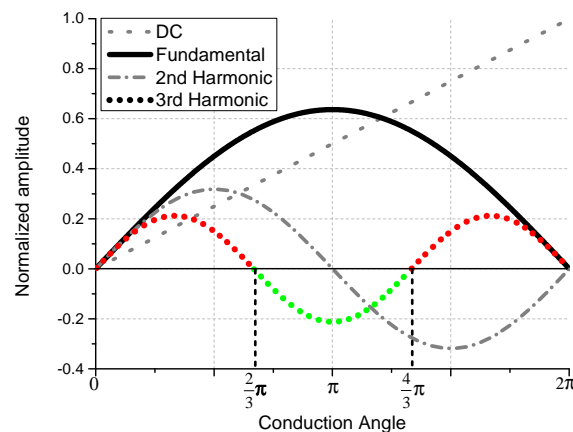


Figure 2. Intrinsic drain current harmonics stimulated by rectangular excitation.

But in order to understand if such an approach, which implies a complexity in the generation of the suitable current shaping, could be helpful in providing better performance with respect to the classic class-F approach (i.e., sinusoidal input and class-AB bias), it is required to analyze the

theoretical performance attainable in the two cases; in particular, the DE and normalized output power level, as reported in Figures 3 and 4, respectively. Specifically, it can be noted that there exists a range of circulation angles, from $\frac{2}{3}\pi$ to $\frac{3}{4}\pi$, highlighted in both figures, where the theoretical attainable DE and power level values exceed the maximum ones achievable in class-AB with the standard approach.

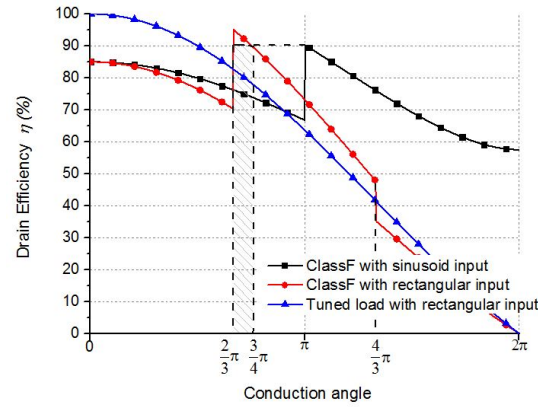


Figure 3. Useful biasing range for class-C-F power amplifier (PA) with respect to drain efficiency (DE).

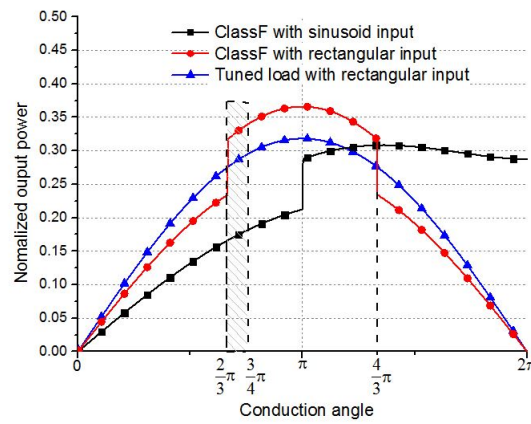


Figure 4. Output power with respect to the useful biasing range of class-C-F PA.

In order to realize a rectangular current wave at intrinsic drain node, a similar excitation must be applied at the input. Nevertheless, the use of a rectangular waveform as the driving signal is not practical, being typically sinusoidal in the signal generated by the external sources. Over-driving the active device is an available solution, taking the advantage of the saturation of the drain current. However, such an approach is unsuitable, since it brings an over-stress of the device itself and an eventual breakdown of the gate junction.

Conversely, the strong non-linearity caused by the class-C biasing point could be used for waveform shaping. In particular, by exploiting the 2nd harmonic termination at the input, it is possible to shape the gate voltage, as in the following [13]:

$$v_{GS}(\theta, h_2) = V_{GG} + V_{G,1} \cdot [\cos(\theta) - h_2 \cdot \cos(2\theta)], \quad (3)$$

where V_{GG} is the gate biasing voltage, $V_{G,1}$ is the fundamental voltage component, and h_2 is the amplitude ratio between the 2nd harmonic $V_{G,2}/V_{G,1}$ and the fundamental components. The 2nd harmonic, which has proper phase and amplitude relationship with the fundamental signal, could realize a waveform with flatness behavior at the maximum value, while peaking the negative value. It would excite a reverse-peaked voltage wave at the gate node, as shown in Figure 5. It is clear that a positive h_2 is needed for this purpose, and the optimum condition raises for $h_2 = \sqrt{2}/4$ [2].

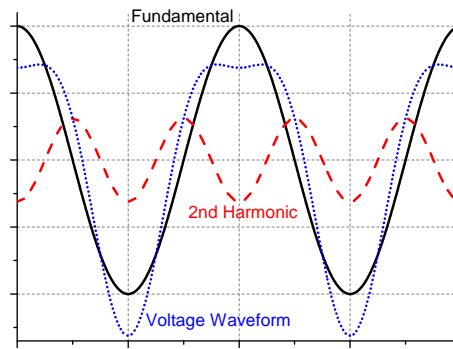


Figure 5. Theoretical gate waveform for class-C-F PA.

Both the class-C biasing condition and the proper 2nd harmonic termination at the input will realize a rectangular-like (better trapezoidal-like) current waveform at the intrinsic drain node. According to the harmonic component analysis discussed previously, a class-F PA design strategy also becomes thus viable in class-C biasing range.

3. Design and Measurements of Class-C-F PA

In order to validate the concepts presented in previous section, a single stage PA centered at 2.4 GHz has been designed and measured, by using the 6 W GaN transistor CGHV1F006s from CREE. The pinch off voltage of the device is -3 V, and its knee voltage is nearly 6.5 V with a drain maximum current of roughly 0.6 A. For the design of the amplifier, the drain voltage was limited to 30 V for practical reasons (i.e., test equipment limitation), while the gate bias voltage was set to -3.5 V. The schematic of the designed amplifier is shown in Figure 6, meanwhile the photo of the realized hardware is shown in Figure 7.

The key point of the class-C-F PA design is to accomplish the gate waveform similar to the ideal one shown in Figure 5 through the proper control of the harmonic impedances at the gate node. In fact, the input matching network (IMN) was designed not only to fulfill the conjugate matching condition at fundamental frequency but also for properly controlling gate voltage by adjusting the 2nd harmonic loading condition. In particular, instead of shorting the latter at the input, as typically done in a tuned load PA design, corresponding to Point B highlighted in Figure 8, it has been modified up to point A, in order to properly shape the intrinsic gate voltage, as shown in Figure 9.

The phase and amplitude relationship between the 2nd gate voltage harmonic and fundamental one has been checked in the design process, in order to maintain a top flattened waveform shaping, as shown in Figure 9. The amplitude of such a ratio (i.e., parameter h_2 as defined in (3)) is reported in Figure 10.

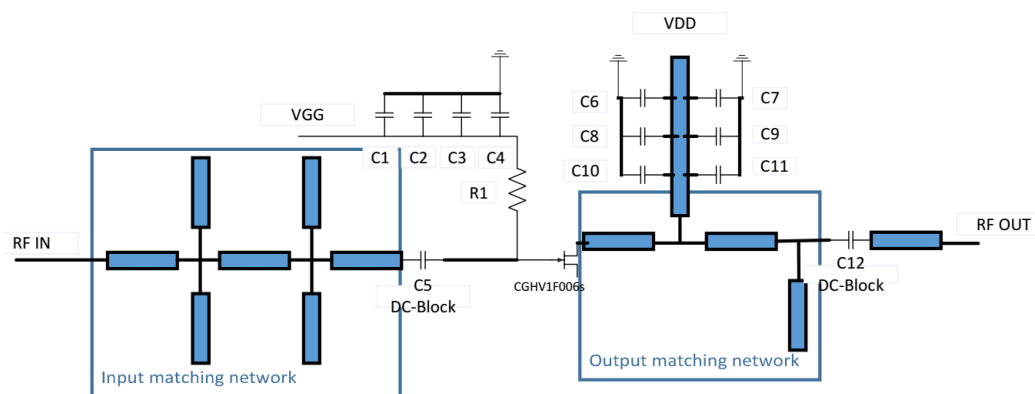


Figure 6. Schematic of the designed class-C-F PA. VGG = Gate Bias; VDD = Drain Bias; RF = Radio Frequency.

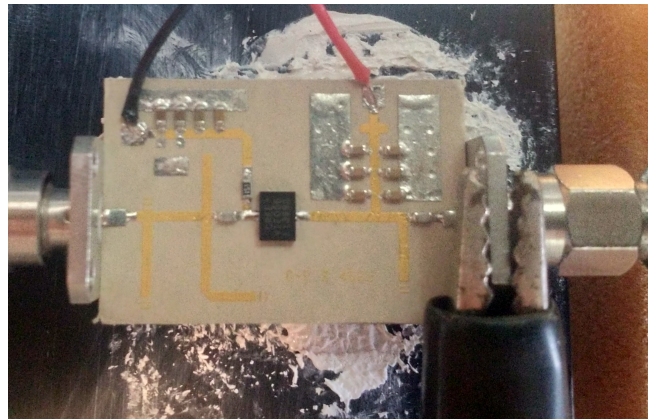


Figure 7. Photo of the realized class-C-F PA.

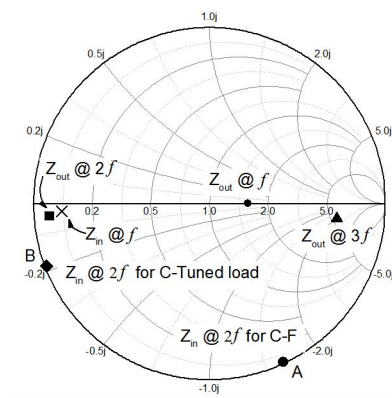


Figure 8. Input (extrinsic) and output (intrinsic) impedance for class-C-F PA.

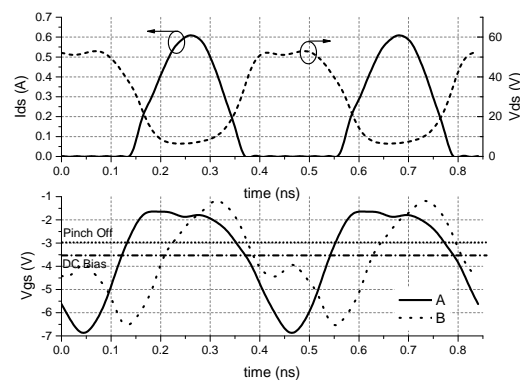


Figure 9. Simulated waveform with respect to the impedance in Figure 8.

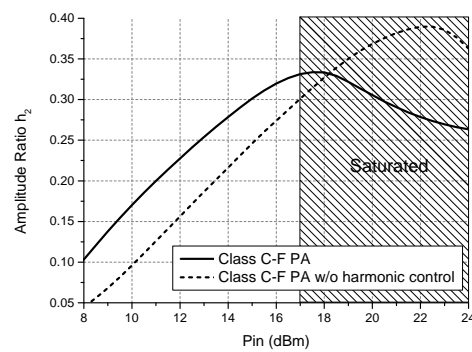


Figure 10. The simulated harmonic amplitude ratio between 2nd harmonic and fundamental frequency at gate node.

Not only is the amplitude crucial but also the phase, since properly phasing the 2nd harmonic can guarantee the flatness behavior of the gate voltage when it achieves its maximum value (see Figure 9). It is to highlight that both amplitude and phase should be carefully monitored. In fact, even if the amplitude of the 2nd harmonic was higher for the loading condition B, after the PA saturation, its phase relationship with the fundamental frequency component would be unsuitable for the required waveform shaping, becoming detrimental to the PA performances, as it will be shown later. Thus, in practical design, both amplitude and phase have to be controlled, eventually compromising the amplitude a little, as presented in Figure 10, where maximum value is quite close to the ideal value of $\sqrt{2}/4$.

The proper input harmonic loading control, together with the strong truncation effect caused by the class-C biasing condition, results in a rectangular-like (or trapezoidal-like) output current waveform synthesized at the intrinsic drain node, as shown in Figure 9. For the design of a class-F PA, the condition of low impedance for the 2nd harmonic and high impedance for the 3rd harmonic of the output voltage was assured through the design of the OMN, also shown in Figure 6. The simulated output loads at the device's intrinsic current source plane are shown in Figure 8.

The load lines resulting from different input/output harmonic terminations are reported in Figure 11, from which it can be highlighted how the proposed approach demonstrates the possibility to design (and realize) a class-F PA biased in class-C, without risking to over-drive the active device.

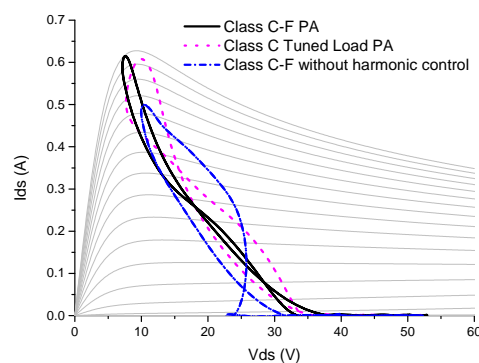


Figure 11. Comparison of simulated load lines among class-C-F PA, class-C-Tuned Load PA, and class-C-F PA without proper gate harmonic control.

The simulated DE, output power, and gain behavior are also compared with the measurement results, as reported in Figure 12a–c, respectively, showing a good agreement. The simulated results of class-C-F PA without harmonic control at the gate node, i.e., with a classical sinusoidal input drive, are also reported in the same figure for comparison.

The realized class-C-F PA performed a peak efficiency of 63% with a saturated output power of 37 dBm (5 W) around 2.4 GHz. Moreover, compared to the attainable performance resulting without harmonic control, the obtained results show the critical role played by phase relationship between the 2nd harmonic and the fundamental one in shaping of the input voltage, allowing the possibility to also exploit such harmonics for a class-C biasing condition.

The results reported in Figure 12d show the performance over frequency range driven by input power 18.4 dBm. An output power over 36 dBm from 2.2 GHz to 2.43 GHz was obtained, with a similar flattening behavior result for the efficiency and gain, which remained close to 60% and 18 dB, respectively, from 2.28 GHz to 2.43 GHz. The dropping behavior is related to the deterioration of harmonic matching at higher frequencies.

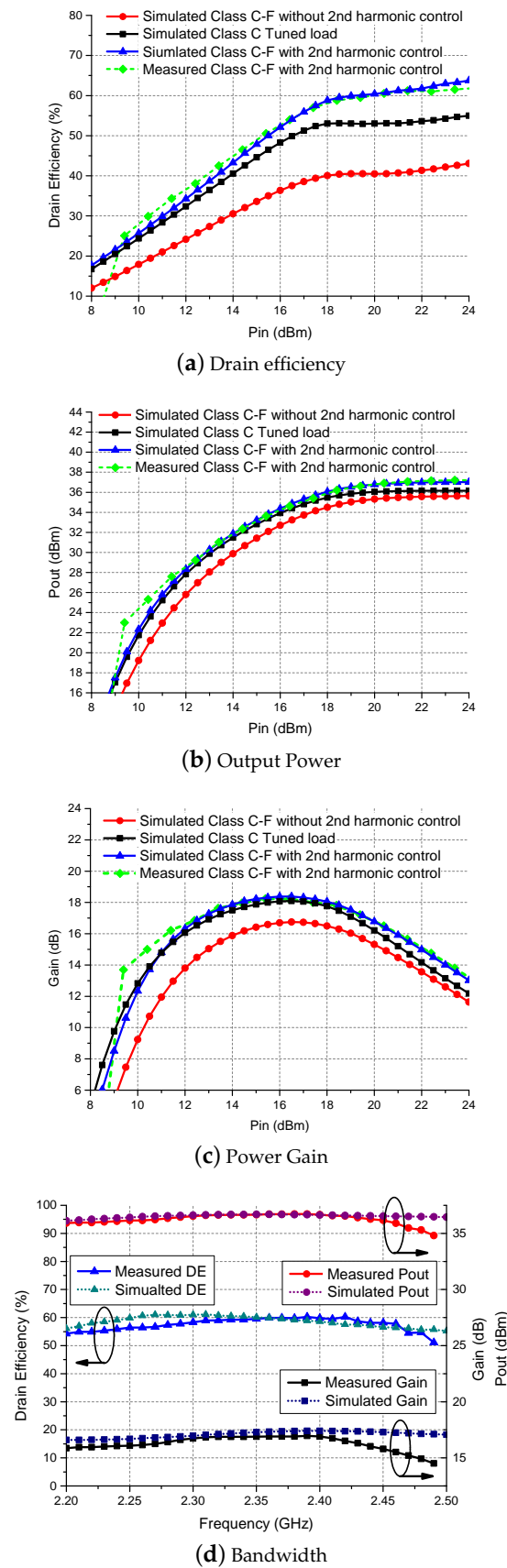


Figure 12. Comparison between simulated and measured drain efficiency (DE) (a), output power (b), and power gain (c) for the designed class-C-F PA, compared with tuned load and improper harmonic control results. Measurement performances over frequency for a fixed input power level of $P_{in} = 18.4$ dBm are reported in (d).

4. Discussion

The feasibility of gate harmonic control adopted to class-C-F PA is validated by the design and measurement results in the previous section. However, there is a crucial aspect that characterizes the present contribution, represented by the class-C biasing condition. In fact, in this case, both the input power level and the gate biasing point have an important role in the waveform shaping.

Different from simulation, a behavior presented in measurement is the slight “trigger” effect at the low input power region, as shown in Figure 12a–c. It is believed that the non-linearity becomes strong enough only after certain input power level (in this case, ≈ 10 dBm) to generate a 2nd harmonic that starts to properly shape the input voltage waveform. The conduction angle is too small to reach the available range for class-C-F PA at low the input power level. Moreover, after the input power level exceeds 12 dBm, the generated 2nd harmonic has the amplitude high enough and the proper phase with respect to the fundamental one, which is sufficient to form a class-C-F PA that has higher DE, output power, and gain than the one biased at class-AB biasing range, as presented in Figure 13. Before that, the waveform of the input signal almost remains sinusoidal, which is unsuitable to drive a class-F PA at class-C biasing range. While in the high input power region, both class-AB-F PA and class-C-F PA reach the same output power and gain level. However, due to the contribution of proper harmonic manipulation, class-C-F PA still achieved higher DE than class-AB-F PA. Figure 14 shows the load lines simulated at the intrinsic of the active device, exhibiting a typical class-F shaping when the input power level is increased.

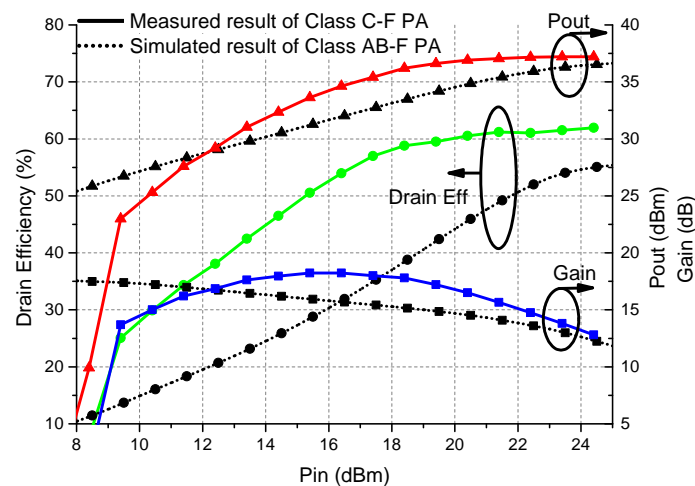


Figure 13. Comparison between simulated class-AB-F PA and measured class-C-F PA.

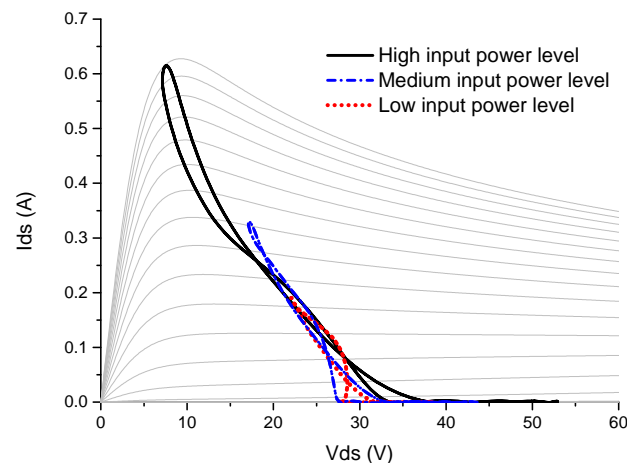


Figure 14. Load lines of class-C-F PA with respect to different input power level.

Another parameter affecting non-linearity is the gate biasing point. A theoretical gate bias range is calculated in Section 2, where it is practically around -3.5 V to -3.9 V. -3.3 V of the gate bias, which is too shallow to generate enough non-linearity; thus, class-C-F PA can only be developed after deep saturation acting like an over-driven PA, as shown in Figure 15.

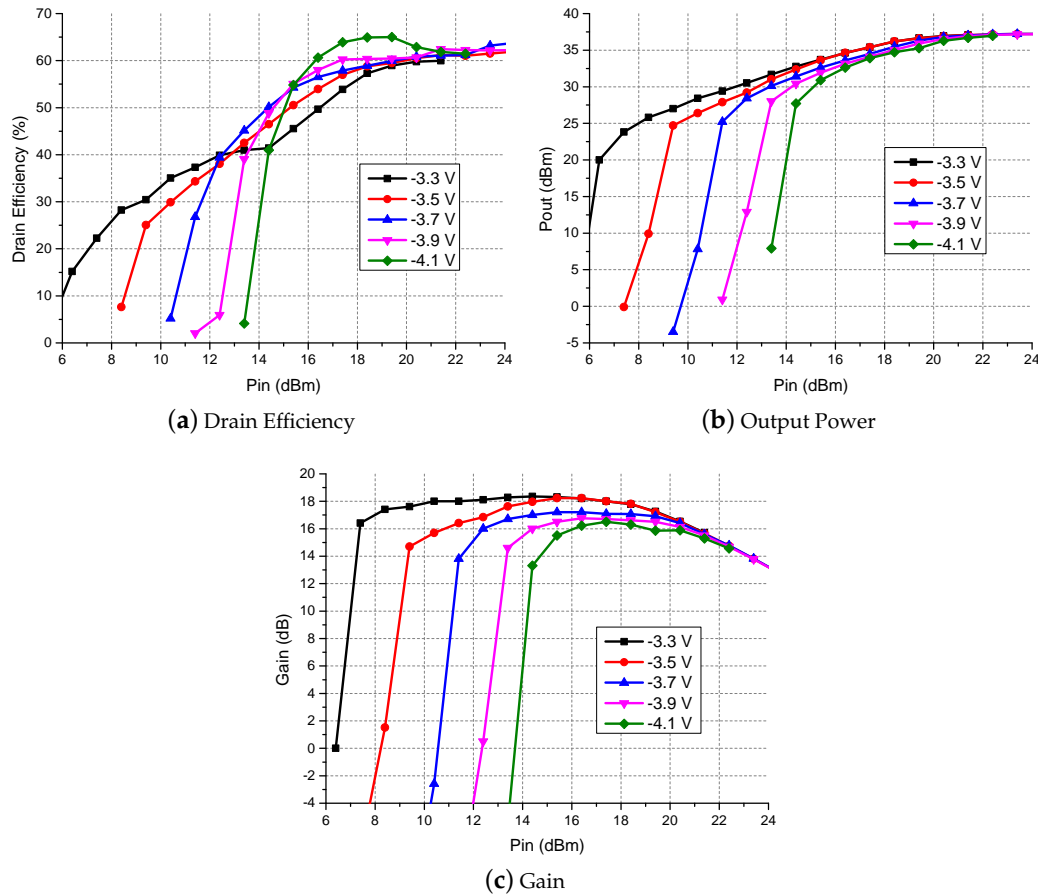


Figure 15. Measured performances of the designed class-C-F PA with respect to different gate bias.

A deeper class-C biasing can result in a higher peak efficiency, as shown in Figure 15a, where for $V_{GG} = -4.1$ V an efficiency level of 66% was registered. However, such a deeper biasing point leads to a less conductive time, which in turn results in a lower output power, as shown in Figure 15b, as well as a lower gain reported in Figure 15c. Moreover, due to the usage of 2nd harmonic at the input, an asymmetrical gate waveform is shaped on the gate junction. Thus, a deeper class-C biasing condition could be risky for the gate junction breakdown itself.

Despite the different gate biases, the PA almost reaches the same DE, output power, and gain in deep saturation, as shown in Figure 15. As it can be noted by the reported experimental measurements, it is clear that from a design point of view that there should be a proper trade-off to balance the desired output power level, gain, and efficiency according to the applications before achieving the saturation by using different biasing sets.

5. Conclusions

In this paper, the concept of gate harmonic control is discussed for the design of a class-C-F PA, validating the proposed approach through the design of a PA with CREE device CGHV1F006s. In particular, in order to avoid issues with a possible device breakdown, the performance of the PA was limited to the maximum power of 5 W. The experimental results demonstrate the possibility to design a class-F PA biased in class-C condition by properly manipulating the harmonics at the input node. Measurements confirmed an output power close to 5 W with a DE higher than 60% (being the overall gain higher than 16 dB) and working bandwidth up to 11% from 2.2 GHz to 2.43 GHz.

The reported theory and experimental results extend the theory of harmonic tuning PA to class-C bias range and proved that harmonic manipulation at gate node is an available method to realize high efficiency PAs. By properly manipulating the 2nd harmonic at gate node, the proper phase relationship between 3rd harmonic and fundamental one at the drain node is obtained, thus realizing a class-C-F PA.

Taking the advantage of the input non-linearity provides more scope for PA designers to balance the performance to satisfy various application scenarios. It is important to set proper harmonic impedance at both input and output in harmonic tuned PA design, especially when the non-linearity is not negligible.

Author Contributions: Writing—original draft and Validation, X.L.; Writing—review, editing and supervision, P.C.; Supervision, F.G.; Supervision, H.Y.; Writing—review, C.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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