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## A 20 mW, 4.8 Gbit/sec, SEU robust serializer in 65nm for read-out of data from LHC experiments

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**ABSTRACT:** The availability of a sub 1-W SerDes for future LHC read-out systems is of paramount importance for building new low-mass inner detectors for HL-LHC. This work reports on the design of two alternative architectures for the serializer block within a high speed transmitter with the objective of achieving a power consumption of less than 30 mW at the operating speed of 4.8 Gbit/sec. Two alternative architectures are implemented using a commercial 65nm LP-CMOS technology. The architectures used are a “simple TMR” and a “code-protected” one, and are meant to investigate different strategies to handle SEUs. While using the same technology and flip-flops, the simple TMR architecture results in a consumption of 30 mW, the code-protected one of 19 mW, which are better than 1/4 of the power used in state-of-the-art rad-hard serializers. Early data on robustness to SEU effects are also presented.

**KEYWORDS:** VLSI circuits; Radiation-hard electronics; Digital electronic circuits

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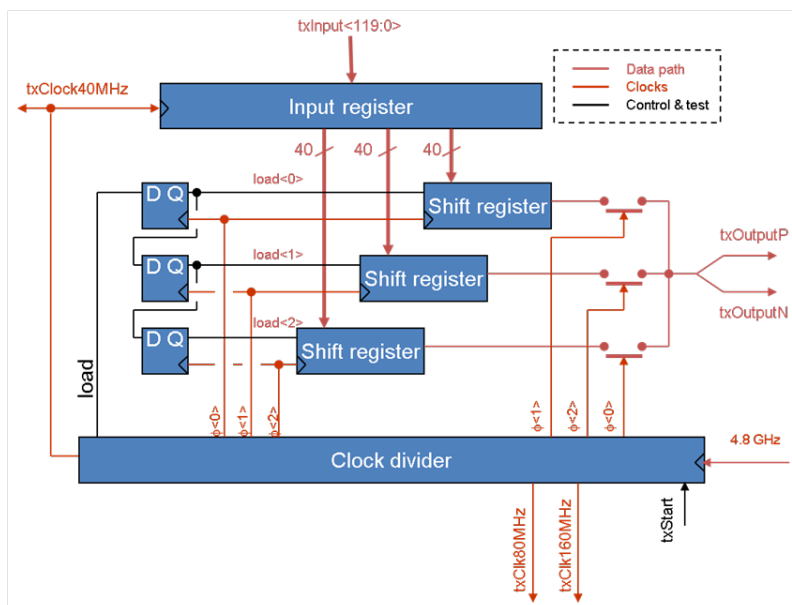
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## 1 Introduction

The availability of a high speed radiation tolerant transceiver with low power consumption is mandatory in a modern high energy physics experiment. Higher beam luminosity is expected with the start of the upgraded LHC (HL-LHC), this means higher data rate produced by the experiments. These data rates require thousands of high speed fiber optics based links, each operating at several Gbit/sec. In addition electronics operating around the LHC experiments require both total ionising dose (TID) and single event upsets (SEU) robustness. Such characteristics are not guaranteed in commercial components. The gigabit transceiver (GBT) was developed at CERN to provide a solution for the communications between the detectors and the control rooms [1]. The GBT was designed in a 130-nm technology and operates at 4.8 Gbit/sec. In order to provide a low power data link to detectors in an increased luminosity environment a new version called low power GBT, or LPGBT, is being designed with a 65 nm LP-CMOS technology.

The high-speed serializer is a fundamental part of a transceiver. The two serializer circuits presented here are designed and characterized as possible solutions for this critical function in the LPGBT. This new block has to satisfy the same requirements of speed of the previous 130-nm version but with a drastic reduction to 30 mW of the power consumption.

In order to implement the same transmission protocol, the word to be sent has to maintain the same structure as in the GBT format. Each word is 120 bit long and it consists of a header and a Reed-Solomon code that can correct up to 4 wrong symbols (4 bit per symbol). To achieve a correction capability of 4 symbols per word, the GBT uses two R-S encoders each with a data correction capability of 2 symbols working in parallel with the symbols from the two encoders interleaved. The new circuit operates with a 1.2 V ( $\pm 10\%$ ) voltage and it accepts CMOS-level data and control signals. The previous version required a supply of 1.5 V. In order to reduce power consumption, various techniques, circuital and architectural, have been used, and they will



**Figure 1.** 130-nm version serializer block diagram.

be illustrated in the following sections. This serializer has to guarantee a tolerance to a Total Ionizing Dose, or TID, of 100 Mrad over ten years of work and it can admit only 1 wrong word transmitted per 24 hours of operation, i.e. a bit error rate of better than  $2 \times 10E - 15$ .

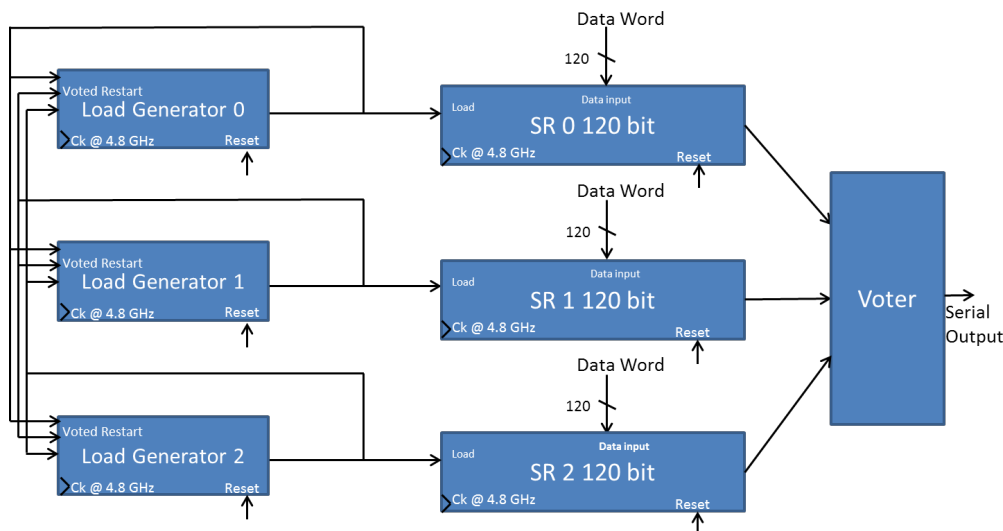
A test chip containing these two serializers was developed and tested to evaluate their performances in a radioactive environment.

The following section describes briefly the serializers and their design. Section 3 explains the test chip architecture, the method used to test the chip and the results of this tests and section 4 summarizes the work.

## 2 Serializer

The 130-nm technology used in the previous version of the GBT does not allow to realize a serializer circuit working at full data rate (4.8 Gbit/sec). Referring to the block diagram of the GBT (see figure 1) it is possible to see its architecture using three different 40 bit shift registers working in parallel at 1.6 GHz with phase shifted clock signals and an output multiplexer to generate the 4.8 Gbit/sec data stream. A clock divider generates also the signal to load the new data word. The flip flops used in this serializer have large channel widths in order to increase the SEU robustness ([2]).

The new 65 nm technology and the lower Vdd used give an intrinsic power advantage which is nevertheless not sufficient to obtain the required reduction. Two solutions have been investigated: a first one called “simple TMR” and a second one called “code-protected”. Both of them use an architecture working at full data-rate and are based on a single 120 bit shift register and a “load generator” logic to update the new data into the final shift register.



**Figure 2.** TMR serializer block diagram.

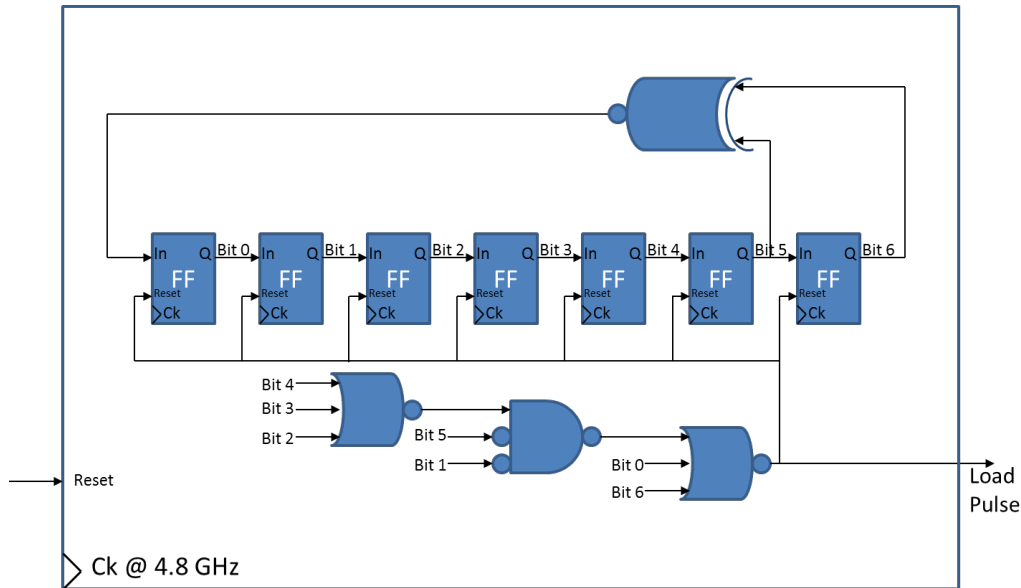
## 2.1 simple TMR serializer

Figure 2 shows the “simple TMR serializer” or TMR SER. The TMR SER uses a triple module redundancy to ensure single event upsets (SEU) robustness, this technique is also used in high reliability applications to protect the system against permanent faults. Three different 120-bit shift registers work in parallel at full 4.8 Gbit/sec speed and are voted at the outputs. Each register has a dedicated load generator logic that generates the load pulse each 25ns. Operation at full data rate requires the use of single phase clock flip flops (TSPC) implemented with low  $V_t$  transistors. The load generator signal (see figure 3) is a very critical part of this design, it replaces the clock divider of the 130-nm version and it has to generate a load pulse synchronously with the shifting clock every 120 clock cycles. A regular synchronous counter would be too slow with a 4.8 GHz clock, so a simpler 7-bit linear-feedback shift register (LFSR) used as a pseudo random counter has been implemented. Figure 3 depicts the logic necessary for the LFSR and the load generator logic.

This 7-bit LFSR counter has to count 120 cycles at line speed, i.e. with a 4.8 GHz clock. To facilitate the time critical function of resetting the counter when reaching its max value of 120, the pattern in the pseudo-random sequence corresponding to its reset value has been chosen carefully as to require a single bit change in the LFSR.

The type of flip flops chosen is the same used in the 130-nm GBT. A comparison between the total size of the transistors in the two technology versions is given in table 1 and illustrates a reduction of  $\sim 52$  times of for the total gate area. This decrease which was made possible by the change of the architecture and strategy to ensure the SEU robustness, assures a considerable power reduction even if the flip flops run at 3 times the speed of the 130-nm version.

The TMR SER can solve the SEU issue, but it doesn’t take full advantage of the Reed-Solomon code that the GBT uses. In fact, in this macro it is used only to protect the possible SEU on the voter.



**Figure 3.** Generic Load Generator block diagram, based on a LFSR counter.

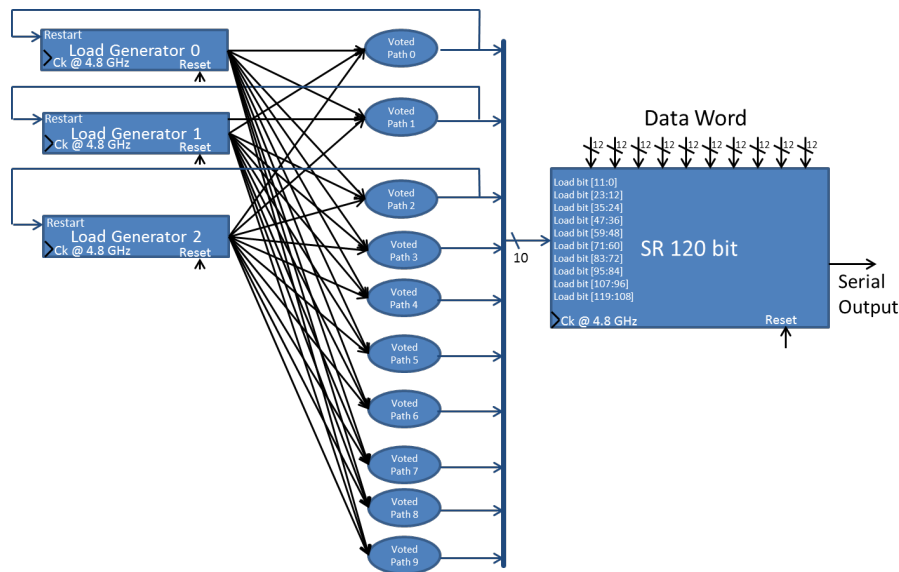
**Table 1.** Comparison between the sizing of transistors in the shift register in the GBT 130-nm version and the 65 nm version

130-nm FF characteristics	130 nm	65 nm
Type	TSPC	TSPC
L (each MOS)	120 nm	60 nm
Total W	170 $\mu\text{m}$	6.6 $\mu\text{m}$
$C_{gate}$	$\sim 11 \text{ fF}/\mu\text{m}^2$	$\sim 16 \text{ fF}/\mu\text{m}^2$
Working frequency	1.6 GHz	4.8 GHz

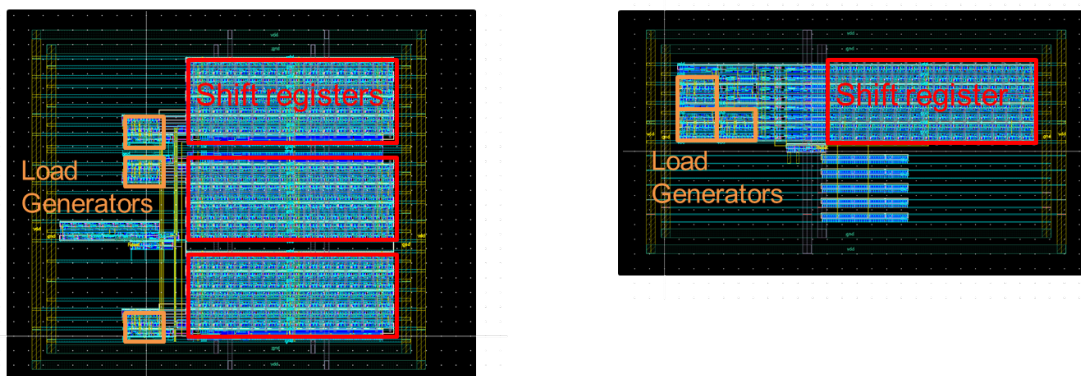
## 2.2 Code protected serializer

The “code protected” serializer, or CP SER, takes maximum advantage of the forward error correction code (FEC) in the GBT protocol. Referring to figure 4, the serializer is implemented as a shift register that operates at 4.8 Gbit/sec. As the data to transmit are R-S coded by a logic block prior to the serializer, potential SEU generated errors on the data path can be corrected at the receiver side. A mixed technique of TMR and coding is adopted instead for the load generation logic. The idea is to split the load control signal in enough branches so that each SEU potentially generated can always be corrected through the Reed-Solomon code. In fact, three load generators are placed like in a traditional TMR, but each output of the generators is used as input of 10 different voters. Each voter generates the load signal for a 12 bit slice of the shift register. A particle hitting one of these voters could upset at most 4 symbols in the word, and the code can still correct errors. This unusual architecture exploits the error correction capabilities of the code to correct SEU both errors in the data path and in the control path.

This circuit was also implemented as a full custom macro based on TSPC flip flops and LFSR counters are used for the load generators. This solution uses a lower number of transistors than the



**Figure 4.** Code protected serializer block diagram.



**Figure 5.** Serializers layouts, TMR SER on the left, CP SER on the right.

TMR SER bringing a further power reduction.

As mentioned above, the LPGBT has to cope with a total ionizing dose of 100 MRad over 10 years. Previous studies (ref. [3]) of TID robustness of the 65-nm technology used have shown that minimum size transistors (in width) exhibit an unacceptable performance degradation after such high exposures. Degradation is instead acceptable if transistors of at least 300 nm width are used, and therefore it was decided to use transistors larger than this size.

The layouts of both serializers is shown in figure 5. The TMR SER occupies an area of  $\sim 7900 \mu\text{m}^2$  while the CP SER an area of  $\sim 3900 \mu\text{m}^2$ .

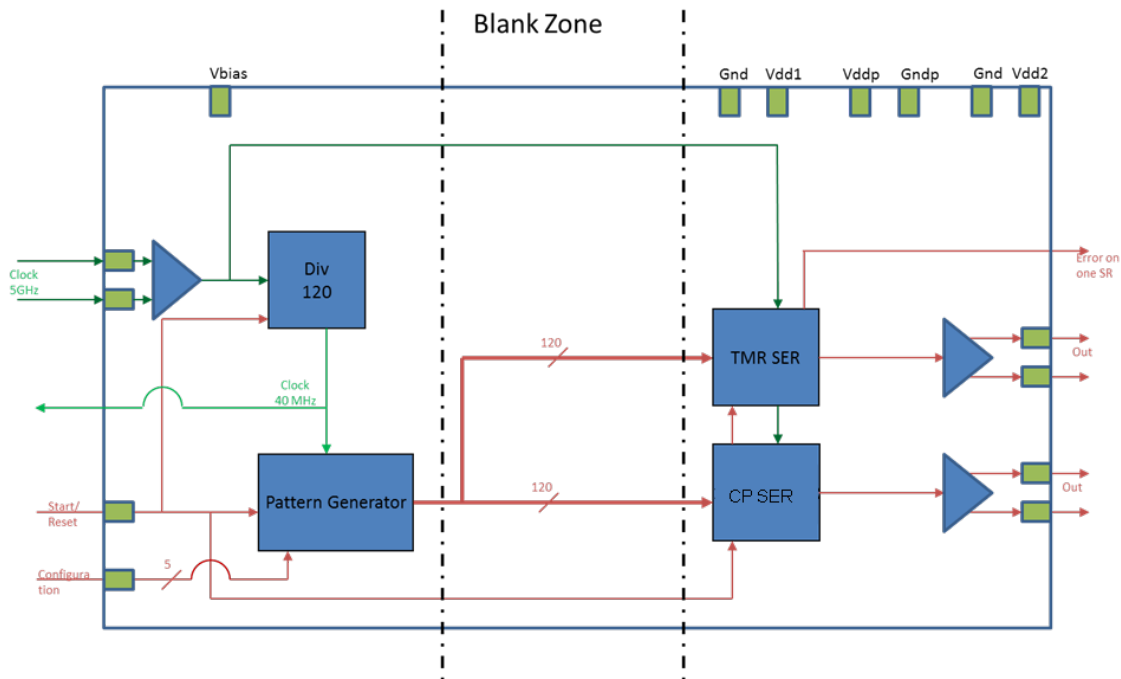


Figure 6. Test Chip block diagram in floorplan.

### 3 Test

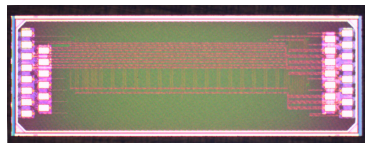
#### 3.1 Test chip

The two serializers have been included in a 3 mm x 1 mm prototype chip and then tested for their functionality and SEUs robustness. The block scheme of the chip is shown in figure 6. The clock signal is provided by an external generator using a differential CML driver. Full custom CML drivers are also used on the test chip to output the high speed signals. The two macros have separated power supply and ground pads in order to permit separate measurements of the power consumption.

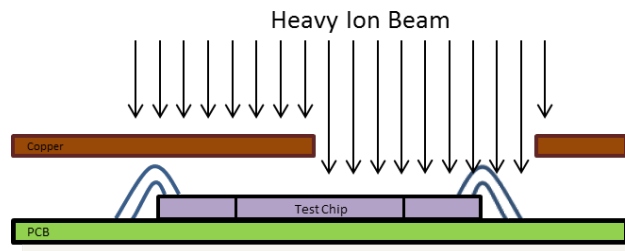
The data words are generated internally every 25 ns with a dedicated pseudo-random generator; a dedicated clock divider is included to provide the 40 MHz clock to the pattern generator. The pseudo-random sequence allows easy external verification.

To facilitate the irradiation and the evaluation of the chip against SEU the chip has been laid out in three sections along the 3 mm direction. The first section of about 0.5 mm contains the clock receivers and the internal pattern generators. This circuitry is not meant to be used in the final chip and is therefore not protected against SEUs. This section of the chip is covered during irradiation with a copper foil of sufficient thickness to avoid penetration of ionizing particles. As it would not have been easy to provide a mechanically precise and sharp shielding of the chip, a second section of about 1.5 mm is then left blank and is meant to be partially covered by the copper shield. This second section contains no critical circuit except for a few clock drivers that have been designed to be SEU tolerant. A third remaining section of about 1 mm length is actually housing the circuitry under study, i.e. the two different serializers. This region is left exposed to the ionizing particles

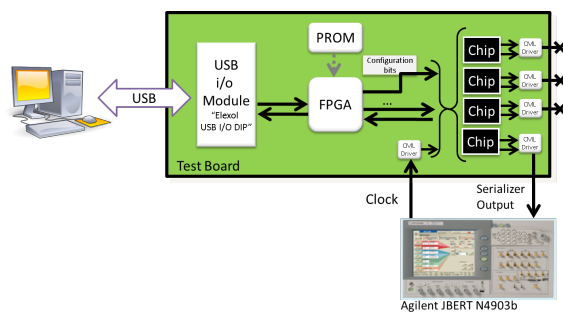




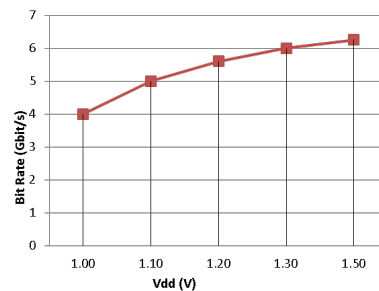
**Figure 7.** Microscope picture of the designed and characterized test chip.



**Figure 8.** Transverse view of the PCB during SEU test and the copper shield placement.



**Figure 9.** Evaluation system.



**Figure 10.** Maximum bit rate vs Vdd, the performances are the same for both serialzier, the two plots are overlaped.

during irradiation. Figures 6 and 8 illustrate this arrangement.

A dedicated custom PCB was developed to evaluate the chip. To increase the SEU cross section during irradiation, 4 different test chips are wire-bonded within the area of the beam spot. The clock signal and the output of each chip are brought on the board or read out through external commercial CML drivers.

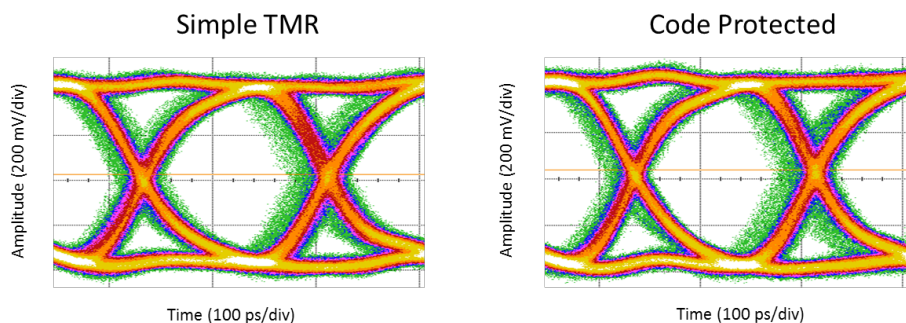
### 3.2 Performance test

The block diagram of the test bench used in the performance test is given in figure 9. The FPGA on the board is used to configure the chip while a Bit Error Rate Tester (BERT) provides the high speed clock signals and compares the output of each serializer with the expected output. Table 2 and figure 10 report the test results in terms of maximum bitrate achievable as a function of the power supply voltage. The maximum speed achieved at 1.2 V is 5.6 Gbit/sec for both serializers. The two serializers show the same data rate performances and both of them match the requirements at the worst supply voltage value of 1.1 V. Figure 11 shows the measurement results of eye-diagrams at 5.6 Gbit/sec and 1.2 V. They refer to the signals read by the BERT at the output of the external CML driver for each serializer. Although these CML drivers will not be part of the final chip, these diagrams are setting an upper limit to the jitter performance of the two serializers (~40 ps for the TMR SER and ~35 ps for the CP SER).

At a frequency of 4.8 GHz and a Vdd of 1.2 V the simple TMR consumes 30 mW whereas the CP SER consumes 19 mW. The measurements on the two serializers confirm the simulations

**Table 2.** Performances test results.

Vdd	TMR SER max bit rate	CP SER max bit rate
1V	4.0 Gbit/sec	4.0 Gbit/sec
1.1V	5.0 Gbit/sec	5.0 Gbit/sec
1.2V	5.6 Gbit/sec	5.6 Gbit/sec
1.3V	6.0 Gbit/sec	6.0 Gbit/sec
1.5V	6.25 Gbit/sec	6.25 Gbit/sec

**Figure 11.** Eye-diagrams of the two serializers at the output of the external commercial CML drivers working at 5.6 Gbit/sec.

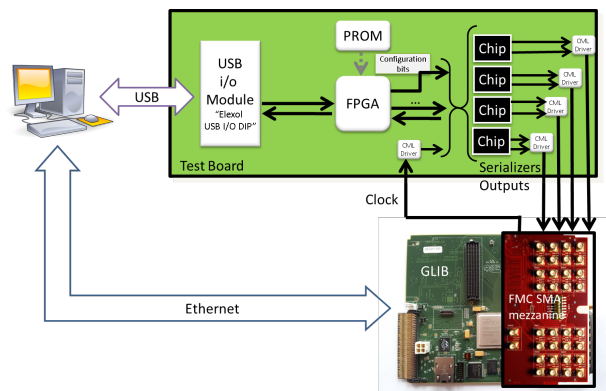
results and satisfy the speed performances and power consumption specifications (4.8 GBit/sec and  $P \leq 30$  mW at  $V_{dd} = 1.2$  V).

### 3.3 SEU robustness test

A heavy ions irradiation test has been performed at the Heavy Ion Facility in Louvain-La-Neuve to evaluate the SEU robustness of the serializer in the HL-LHC environment. Figure 12 shows the testbench used. This testbench is similar to the previous one (figure 9) but the commercial BERT is replaced by a GLIB board ([4]) based on a Virtex-6 FPGA that implements the same function of the JBERT but reads all four different chips outputs while they are irradiated.

The first test at the Louvain heavy ion beam has been partially inconclusive because of a bug in the read-out FPGA. Nevertheless, what could be determined were the following facts:

- both serializers have exhibited some single bit errors, all of which are correctable anyway by a receiver implementing the proper RS decoder algorithm
- the CP serializer also have exhibited some block errors (for blocks shorter than 16 bits), again which can be corrected entirely by a proper RS receiver
- some rare errors with a large number of incorrect bits have also been observed, more precisely 4 wrong words for the TMR SER and 9 wrong words for the CP SER have been observed over a total fluence of  $6.6 \times 10^7$  ions/cm<sup>2</sup>. This errors have amounted to a bit error rate probability of  $1.65 \times 10^{-3}$  wrong words/day for the TMR SER and 1.7 wrong words/day for the CP SER. Such errors also have caused the FPGA to misbehave. It is to be noted that



**Figure 12.** SEUs testbench, the bert has been replaced by a GLIB board.

the cause of such errors is not well understood and that they could actually be artifacts of the test system used. For instance, the shielding of the auxiliary circuitry on the chip can not be fully guaranteed and such errors could disappear with some simple modification of the test setup.

An additional test, capable to collect more detailed data, is being prepared where the final cross section measurements will be made and the cause of these unexpected error configurations will be investigated.

#### 4 Conclusions

A low power serializer macro has been realized in two versions in 65 nm technology for a future GBT tranceiver for HL-LHC. In the “code protected” serializer a way to extend the use of forward error correction code to protect the behaviour of the control logic as well as the data path is introduced.

Both serializers are functional and the power consumption and bitrate measurements are according to the simulation results. The TMR version satisfies the SEU robustness specifications and consumes  $\sim 37\%$  more power than the Code Protected version. The CP SER error rate is marginally over the SEU requirements (1 wrong word/day) and a new test is being prepared to conclusively measure the error cross sections for both versions. The robustness to total dose is also going to be verified and compared to expectations.

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- [4] P. Vichoudis et al., *The Gigabit Link Interface Board (GLIB) ecosystem*, [2013 JINST 8 C03012](#).