Neutron-Induced Upsets in NAND Floating Gate Memories

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***Abstract*—We investigate atmospheric neutron effects on floating-gate cells in NAND Flash memory devices. Charge loss is shown to occur, particularly at the highest program levels, causing raw bit errors in multilevel cell NAND, but to an extent that does not challenge current mandatory error correction specifications. We discuss the physical mechanisms and analyze scaling trends, which show a rapid increase in sensitivity for decreasing feature size.**

***Index Terms*—Flash memories, floating gate, neutrons, soft errors.**

I. Introduction

THE FIRST time that soft errors were mentioned was in 1962, when Wallmark and Marcus predicted that atmospheric neutrons could put an end to CMOS scaling at a feature size of 10 μm [1]. Soft errors at sea level, originating from scattered particles in the atmosphere or alpha-emitting contaminants in chip materials, are a known source of disturbances in SRAMs and, to a lesser extent, in DRAMs [2]. Relatively less is known about the sensitivity of Floating Gate memories, one of the most pervasive type of memory. An extensive literature covers the effects of heavy ions [3]–[8] and total dose [9], [10] on FG cells, but little data obtained with particles matching the terrestrial neutron environment are available [11]–[14].

In general, technology scaling is bringing about devices where smaller and smaller amounts of charge are used to store information, which could make them increasingly sensitive to ionizing radiation. Actually, the scenario is more complicated than that. For instance, even though less charge is required to upset a more scaled SRAM cell, the cell area reduction causes the charge collection efficiency to diminish with shrinking feature size. As a result, experimental data on SRAMs show a constant bit error rate as a function of the feature size [2], or even a decrease starting from the 90-nm node [15]. This trend must be coupled with the tendency to include an increasing amount of memory in integrated circuits, usually resulting in a growing chip (system) sensitivity to atmospheric neutrons and alpha particles [2].

The reduction in storage charge is particularly evident in state-of-the-art NAND Flash with Multilevel Cell architectures, where only few hundred electrons separate two contiguous levels. In these memories, the loss (or trapping) of just a few carriers due to ionizing radiation can easily upset a bit. NAND flash memories require the use of Error Correction Codes (ECC) because they are affected by a number of phenomena that lead to non-zero bit error rate: program disturb, quantum-level noise, erratic tunneling, stress induced leakage current, read disturb, and detrapping-induced retention issues [16].

The purpose of this work, which is an extension of [14], is to understand whether atmospheric neutrons can be a significant source of bit errors in Flash memories. As we will see, the results are very reassuring: the atmospheric neutron threat is well under control. The paper is organized as follows: Section II details the features of the devices used in this work. Section III presents the experimental results obtained exposing Flash memories to neutrons. The simulation results on the interactions of neutrons with the chip materials are illustrated in Section IV. Section V discusses the main factors determining the neutron sensitivity of floating gate memories.

II. Experiments and Devices

Throughout this work we used commercial Single Level Cell (SLC) and Multilevel Cell (MLC) NAND Flash memories. The feature size of the tested devices ranges from 90 nm to 48 nm (Table I). In Numonyx samples, measurement of the cell threshold voltage ($\mathrm{V_{th}}$) was possible thanks to the availability of reserved test modes. On the other sets of samples, only the number of raw digital errors was measured (without the application of any error correction code). In the following, the cell levels in the MLC chips are numbered from the lowest to the highest $\mathrm{V_{th}}$ as L0, L1, L2, L3.

Irradiation was performed at the VESUVIO line of the ISIS facility at the Rutherford Appleton Laboratory, in Didcot, U.K., using a wide-energy neutron beam. The VESUVIO neutron spectrum reasonably reproduces the terrestrial environment, with several orders of magnitude of acceleration [17], [18].

Devices were measured before and after irradiation, and left unbiased at room temperature during the exposure to neutrons.

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TABLE I
DEVICES USED IN THIS WORK

Manufacturer	Architecture	Feature size [nm]	Capacity [Gbit]
A	NAND MLC	90	8
A	NAND MLC	65	4
A	NAND MLC	51	32
B	NAND MLC	65	8
B	NAND MLC	50	32
Numonyx	NAND MLC	60	8
Numonyx	NAND MLC	48	16
B	NAND SLC	90	4
A	NAND SLC	65	4
Numonyx	NAND SLC	48	1

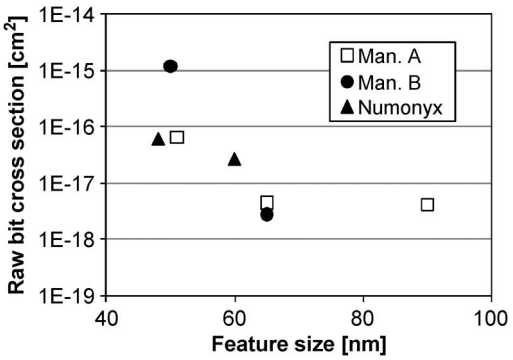

Fig. 1. Cross section for raw bit errors induced by wide-spectrum neutrons in MLC NAND cells programmed at L3 in Flash memories from different manufacturers. Thousands of events were collected for each point. Error bars are smaller than the symbols (95% confidence intervals).

Unirradiated reference devices were kept alongside the irradiated ones and measured at the same time.

The Los Alamos Neutron Science Center (LANSCE)-equivalent neutron fluence above 10 MeV on the samples was in the order $2 \cdot 10^{10}$ n/cm^2 in each of the measurement shift, corresponding to more than 150 000 years at New York City. The LANSCE-equivalent flux can be used to compare the experimental data obtained at the ISIS facility with those at LANSCE [19], the facility that comes the closest to matching the JEDEC JESD89A [20] reference spectra. This correlation is necessary, because ISIS-VESUVIO features a different spectrum than LANSCE.

III. EXPERIMENTAL RESULTS

Fig. 1 shows the raw bit cross section (i.e., with no error correction codes), σ, of errors attributable to neutrons, as a function of the feature size for bits programmed at the highest level (L3) in MLC NAND Flash memories. The bit cross section is defined as the number of errors divided by the fluence and by the total number of bits. Fig. 2 illustrates the dependence of the cross section on the program level. The most affected bits are those belonging to the two highest levels, L2 and L3.

σ increases more than one order of magnitude in two generations for manufacturer A. The cross section for the smallest feature size is less than 10^{-16} cm^2, a factor of 100 smaller than

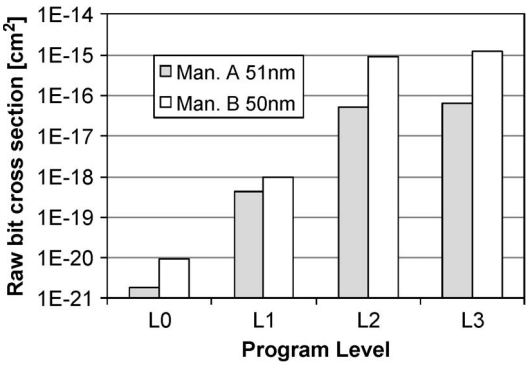

Fig. 2. Cross section for raw bit errors as a function of the program level for two of the tested memories.

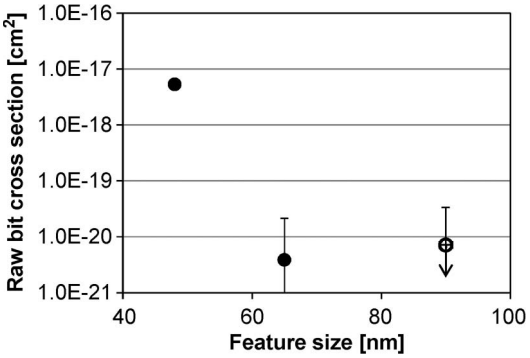

Fig. 3. Cross section for raw bit errors induced by wide-spectrum neutrons in SLC NAND. The memories are produced by different vendors (Table I). No errors have been observed on 90-nm parts, the reported value is an upper bound based on the number of tested cells and neutron fluence. Only one error has been measured on the 65-nm parts, which gives a large uncertainty on the result. On the contrary hundreds of events have been measured on 48-nm parts, with error bars smaller than the symbol.

that for a typical SRAM cell [2], [21]. The increase from one generation to the other is stronger in manufacturer B, more than three orders of magnitude. The absolute value of σ is higher in manufacturer B, as well, at 10^{-15} cm^2, for the worst-case pattern and smallest feature size. In all cases, the upsets are from one level to the adjacent one with lower $V_{\rm th}$.

σ can be used to calculate the raw bit error rate on the field for a certain location, using data on the neutron flux. Assuming a value of 13 n $\cdot$ cm^{-2} $\cdot$ hour^{-1} at NYC [20], the raw bit error rate due to atmospheric neutrons over a period of ten years in the worst case (Vendor B, L3) is $1.13 \cdot 10^{-9}$. This value is comparable to other mechanisms of bit errors [16]. The uncorrectable bit error rate is the probability that more errors will be generated in an ECC codeword than can be corrected. Assuming an ECC scheme capable of correcting 8 bits and an ECC codeword of 539 bytes, as prescribed by the manufacturer datasheet, the uncorrectable bit error rate will be, according to the binomial distribution, much less than $1 \cdot 10^{-18}$. At avionics altitudes, the neutron flux can be 300 times higher, resulting in a worst-case raw bit error rate of $3.4 \cdot 10^{-7}$, which, translated into uncorrectable bit errors, is still well below $1 \cdot 10^{-18}$. The other tested memories exhibit lower raw bit error rates.

Fig. 3 shows the sensitivity of SLC NAND Flash memories to neutrons. The three memories are produced by different manufacturers (Table I), which makes the comparison between

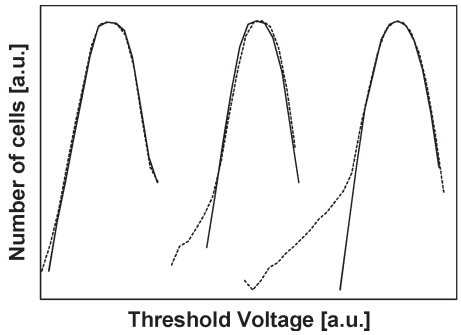

Fig. 4. Threshold voltage distribution for a 60-nm MLC NAND Flash memory irradiated with wide-spectrum neutrons. Dashed lines are post-rad.

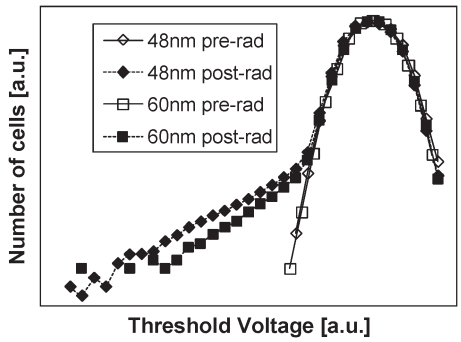

Fig. 5. Comparison between the threshold voltage distributions before and after wide-spectrum neutron irradiation for two MLC NAND Flash memories with different feature sizes.

different feature sizes somewhat less precise. Only the program state has been considered (the erase level is not sensitive). At a feature size of 50 nm, the raw bit cross section is one or two orders of magnitude below that of MLC devices. An increasing trend with scaling is visible, but we collected just a handful of events in the 65-nm parts, so no conclusion can be drawn about the real magnitude of the increase due to this large uncertainty.

V_{th} distributions were measured, in addition to the number of errors, before and after neutron irradiation in the set of NAND samples from Numonyx. Increasingly longer tails appear in the distributions (Fig. 4), for increasing cell V_{th}. Fig. 5 compares the V_{th} distributions before and after irradiation for two different technology nodes. The two devices were irradiated with the same fluence ($1.68 \cdot 10^{10}$ n/cm^2), so it is apparent how both the number of cells in the tail and the maximum V_{th} shift increase with decreasing feature size. These tails are not permanent, in the sense that an erase/program cycle restores the correct threshold voltage distribution.

IV. Geant4 Simulations

We developed an application based on the Geant4 toolkit [22] to simulate the interactions of neutrons with the chip materials. Geant4 is a collection of C++ classes, which contains a variety of utilities and physics processes to model the interaction of radiation with matter. It includes both electromagnetic and hadronic interactions.

The geometry and materials of the Numonyx samples were modeled in detail in three dimensions. A 2-D drawing of the

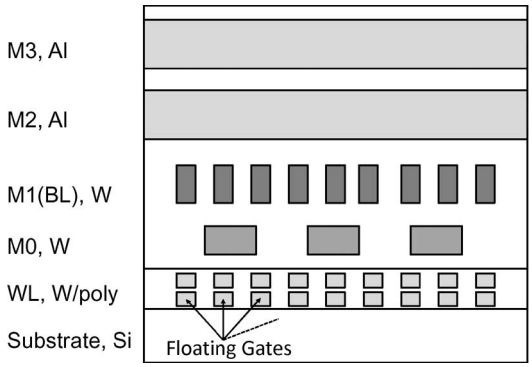

Fig. 6. Drawing (not to scale) of the structure simulated for the assessment of neutron byproducts. WL = Wordline, BL = Bitline, Mx = Metal x. M0 is present only in 48-nm parts.

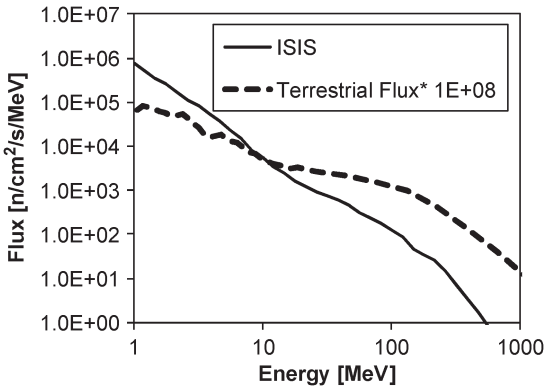

Fig. 7. Neutron ISIS spectrum as compared to the IEC reference [10] multiplied by a factor of 10^8.

examined structure (not to scale) is shown in Fig. 6. The ISIS neutron energy spectrum (Fig. 7) was also carefully reproduced in the simulations.

The output of the simulations are the number, species, energy, and trajectory of the particles that cross the floating gates depositing energy along their paths. An event is defined in the following as the deposition of energy inside a FG.

To reduce the variance on the rarest events (i.e., those produced by high-energy neutrons), the low- and high- energy parts of the ISIS spectrum were simulated separately. This allowed us to reduce the total amount of events to be simulated, while producing enough high-energy neutrons events to obtain accurate statistics for rare events. Afterwards the results were combined, applying the proper weight (given by the ratio between high- and low-energy neutrons in the ISIS spectrum) to the results coming from the different simulations.

Geant4 treats energy deposition by ionization as the sum of a continuous deposition and discrete events, whose production depends on the range cut set by the user. When the ionization process produces electrons whose range is above the cut, these electrons are tracked, otherwise the energy deposition associated with them becomes part of the continuous component. The range cut for electrons was set as small as possible, so that energy deposition in the FG is assessed not only for ions directly crossing the FG, but also for particles passing close enough to generate electrons that can reach the FG.

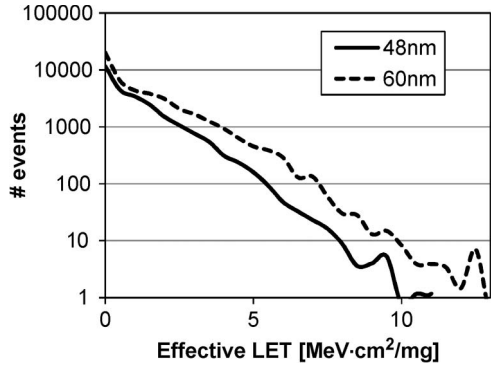

Fig. 8. Simulated distribution of neutron-induced secondary particles LET in 60-nm and 48-nm parts.

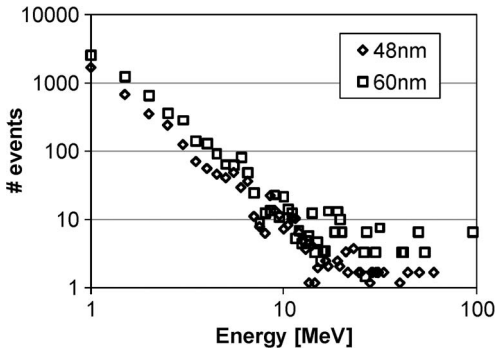

Fig. 9. Simulated distribution of neutron-induced secondary particles energy in 60-nm and 48-nm parts.

Fig. 8 shows the number of the secondary particles crossing the FG as a function of the effective LET for the 48-nm and the 60-nm Numonyx parts, considering an equal number of cells and the same neutron fluence on both parts. The effective LET was calculated as the deposited energy divided by the density of silicon and by the FG thickness. Because of the larger geometrical size, the total number of events (the integral of the curves in Fig. 8) is larger in the 60-nm parts than in the 48-nm ones. The shapes of the two curves are different because of the different thicknesses of the materials the particles cross before reaching the floating gate. As seen in Fig. 8, the distributions are approximately linear in a log-lin scale and the maximum LET is around 10 MeV $\cdot$ cm^2/mg for both technologies. The smallest LET bin, below 1 MeV $\cdot$ cm^2/mg, contains a lot more particles than the other bins, due to the large amount of generated protons and alpha particles. These lighter particles can travel a longer distance than those with higher LET, which lose their energy faster along the way.

Fig. 9 shows the energy distribution of the particles with LET above 1 MeV $\cdot$ cm^2/mg produced by the neutrons. Particles with LET below 1 MeV $\cdot$ cm^2/mg were not included in the analysis, as they give only a marginal contibutions to the number of upsets, as shown in the following. As seen, the energies are fairly limited: most of the particles are below 10 MeV. This is an important aspect, because the structure of the e-h track generated by the ions is dependent on the energy, in addition to LET [23]. Furthermore, low energies mean that the neutron-triggered events are not likely to affect many bits, and that long tracks of adjacent FG cells experiencing charge loss (such as those observed in [24]) are unlikely with neutrons. We must

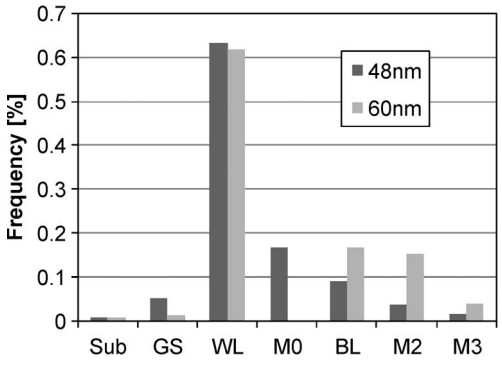

Fig. 10. Simulated origin location distributions of the neutron byproducts with effective LET $>$ 1 MeV $\cdot$ cm^2/mg crossing floating gates in 48-nm and 60-nm Numonyx parts. Sub = Substrate, GS = Gate stack, WL = Wordline, BL = Bitline, Mx = Metal x. Each layer contains also the isolation up to the next layer going from the substrate to the passivation. Note that M0 is not present in 60-nm parts.

remark, though, that we only simulated the conditions found in our experiments—in particular, normal incidence. It may be possible that with different angles, multiple effects occur, because the directions of the secondaries are a function of the impinging neutron direction.

Another interesting correlated aspect is shown in Fig. 10, which reports the locations in the chip where ionizing secondaries originate during exposure to neutrons. Most of the events are due to particles generated in the proximity of the worldlines, whereas as expected, the other layers give a decreasing contribution as their distance from the floating gate increases. The events come for the most part from the oxide isolating the wordlines, rather than from the wordlines themselves.

Our simulation results show that the largest part of the events is due to reactions between neutrons and Silicon or Oxygen atoms. Events with Tungsten and other heavier materials in the back-end are much more rare, and contribute to the total neutron-induced number of events for less than 1%.

V. Discussion

As we have discussed in the previous section, neutrons interact with chip materials through elastic or inelastic nuclear reactions that generate charged secondary particles (heavy ions). These byproducts can cross (or pass nearby) FG's, inducing charge loss [25] and, to a lesser extent, charge trapping in the oxides surrounding the FG [26]. This translates into a shift in the threshold voltage of the hit cells, which, when large enough to take the cell beyond the reference voltage, causes a raw bit error. Obviously this is not enough to cause an error visible to the user, because mandatory ECC schemes have to be implemented by the application in the case of NAND devices.

A. Scaling Trends

A clear trend toward an increasing error rate for decreasing feature size is visible in our experimental results. NAND MLC are the most sensitive among the studied devices (Figs. 1 and 3). *In fact,* the smaller read margin make MLC more sensitive than SLC. In the following we will therefore focus only on NAND MLC.

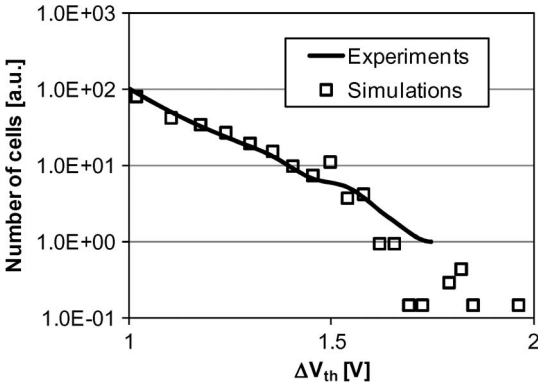

Fig. 11. Comparison between experimental neutron-induced tails and weighted simulations of energy deposition in 60-nm parts.

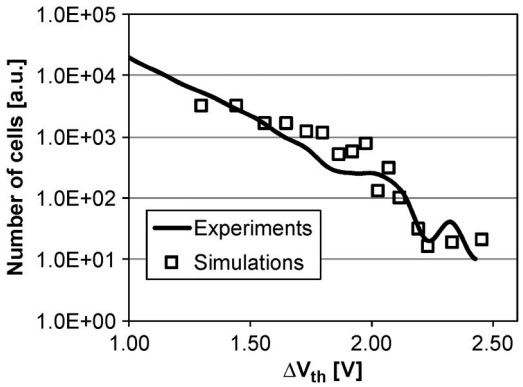

Fig. 12. Comparison between experimental neutron-induced tails and weighted simulations of energy deposition in 48-nm parts.

The tails in Figs. 4 and 5 are approximately linear in a log-lin scale, meaning that the distribution of threshold voltage shifts induced by neutron byproducts is exponential. This distribution arises from the fact that the generated secondaries have a wide spread in energy, range, and LET. To match the experimental data (Figs. 4 and 5) with the simulated events (Fig. 8), we need to establish a relation between the LET of the generated particles and the threshold voltage shift experienced by the cells. In doing so, we neglect the impact of the impinging particle energy, which is anyway a second-order factor. The correspondence between $\Delta V_{\rm th}$ and LET is done as follows: if there are n cells experiencing a threshold voltage $\Delta V_{\rm th}$ and n cells in our simulations hit by particles having a linear energy transfer LET, we assume that LET produces $\Delta V_{\rm th}$. For this purpose we used a power law, where we chose the pre-factor (A) and the exponent (B), by fitting the data on the basis of the number of events

$$\Delta V_{\rm th} = A \cdot LET^{B}. \tag{1}$$

The results are shown in Figs. 11 and 12, where A is equal to 0.8 and 1.2 and B to 0.35 and 0.3 for 60-nm and 48-nm parts, respectively. A linear relation, which was assumed in previous works [27], between $\Delta V_{\rm th}$ and LET does not provide a good fit for the data. Yet, (1) is only an approximation, because, as shown in the past, LET is not the only parameter that determines $\Delta V_{\rm th}$. In fact, the impinging particle energy plays a fundamental role as well [23]. Following the arguments of [23], a lower energy ion produces a track with a smaller diameter, because of the lower energy of the delta electrons emitted normal to the ion trajectory, and this translates into a higher threshold voltage shift, because of the higher conductivity of the transient conductive path.

As we mentioned, errors take place only if the threshold voltage shift is large enough, that is to say, only if the LET of the impinging particle is above a certain threshold LET $(\mathrm{LET_{th}})$. With our approach we can estimate the $\mathrm{LET_{th}}$ for the two devices, by simply looking at the number of errors. The results are ~ 2 MeV $\cdot$ cm^2 $\cdot$ mg^{-1} for 60-nm parts and ~ 0.5 MeV cm^{2}mg^{-1} for 48-nm devices. These numbers are in agreement with published heavy-ion data [14], confirming the correctness of the approach.

These considerations justify the observed scaling trend: the beneficial impact of the reduction in cell area is more than offset by the decrease in threshold LET. The rapid increase in cross section with decreasing feature size can be explained considering as follows:

- the total number of events depends on the cell area, i.e., it is quadratically dependent on the feature size (Fig. 8);
- the number of events versus LET is exponentially distributed (Fig. 8);σ can then be expressed as

$$\begin{aligned}\sigma &= k_1 F^2 \int_{LET_{\rm th}}^{+\infty} \exp(-k_2 LET)\, dLET \\ &= \frac{k_1}{k_2} F^2 \exp(-k_2 LET_{\rm th})\end{aligned} \tag{2}$$

  where F is the feature size and k_1, k_2 are constants.
- to a first order, the threshold LET is a function of the ratio between the stored charge and the charge deposited by the heavy ion. This ratio depends quadratically on feature size

$$\begin{aligned}\sigma &= \frac{k_1}{k_2} F^2 \exp\left(-k_2 \frac{F^2}{k_3}\right) \\ &= k_A F^2 \exp\left(\frac{k_B}{F^2}\right)\end{aligned} \tag{3}$$

  Equation (3) is valid only if the cell charge collection efficiency, defined as the amount of charge released by heavy ion that causes charge loss in the FG, is constant with feature size. In other words, (3) is valid under the hypothesis that the particle-generated track is contained inside the FG volume. When cells are shrunk, this may no more be the case, strongly mitigating the rapid growth predicted by (2).

B. Materials, Margins and Electric Field

Although neutron nuclear interactions with Si and O are by far the most common, byproducts originating from reactions with high-Z materials employed in the CMOS flow (such as Tungsten) can be very important in certain situations [28], because they generate high-LET particles. However, our simulations show that these reactions account for only a very small number of events. They might have been significant a few generations ago, when the threshold LET for an error was far higher, so that these events were the only ones able to produce

an error. Given the relatively low threshold LET necessary to produce an error that we estimated earlier, changes in materials (for instance the replacement of Tungsten) in future technology nodes are not expected to play a major role on the sensitivity to neutrons (as long as Silicon and Oxygen will be the two most common materials).

In principle, all the analyzed MLC NAND memories from the three manufacturers share the same architecture, so it is at first surprising to see large differences (Fig. 1) of more than one order of magnitude in the raw bit error rate at a feature size of $\sim$50 nm. Differences in the materials surrounding the FG or in the back-end can alter the spectrum of particles impinging on the FG. Yet, this does not appear as the main driving factor, as the particles mainly responsible for upsets are silicon and oxygen, and the concentration of those materials should not vary significantly across different manufacturers. It is more likely that the spectrum of particles generated by neutrons is roughly the same in all the devices, but the FG sensitivity changes (i.e., the threshold LET), even for nominally identical feature sizes, due to different read window margins. In fact, because of the exponential shape of the events versus LET curve (Fig. 8), even a small change in threshold LET can turn into a large change in the error number.

The dependence of charge loss on the electric field (E) has been investigated in detail for heavy ions. A larger E increases the discharging current triggered by the heavy ion [27]. This translates into a higher charge loss, and explains very well the program level dependence of our data. In an alternative view, the electric field modulates the transient carrier flux across the oxide barriers, impacting the amount of charge loss [11]. In addition to the data on the raw single bit sensitivity (Fig. 2), this dependence is evident also on the $V_{\rm th}$ distribution of Fig. 5, where a longer tail appears on the highest program level. The lowest program level and the erased level are practically immune from errors. The fact that the neutron sensitivity increases with the electric field is somehow helpful to design ECC schemes. The reason is that several other factors that affect reliability tend to have the same dependence on E. In this way, a custom ECC designed to exploit the level dependence can efficiently act also for neutron–induced errors.

No scaling is in sight for the electric field, at least as long as the floating-gate architecture will be maintained. Therefore, no reduction (nor increase) of the neutron sensitivity can be expected due to changes in the electric field.

In addition to the sensitivity of the floating gate array, one should also consider the effects in the peripheral circuitry. In fact, the read-out protocol of NAND memories includes the transfer of data from the floating gate matrix to a temporary storage, called page buffer. This page buffer is an array of latches, which in principle is susceptible to soft errors [25]. The microcontroller that manages the operation of the Flash memory contains state information, which can be upset by radiation [25]. Furthermore, Single Event Transients (SET), can originate in combinational or analog blocks.

These errors have been observed with heavy ions, but, so far, not with neutrons. However, the heavy-ion data are reassuring: high-LET ions are needed to produce these events [25]. This is due to the fact that the NAND periphery is realized using thick oxides for cost reasons (fewer masks), and large cells, which therefore do not mirror the scaling trends of SRAM cells and logic circuits with respect to soft erorrs.

VI. Conclusion

We showed that neutrons can induce raw data loss in FG memories, especially in MLC devices. The neutron raw bit error rate increases with decreasing feature size for all types of FG devices. This is a consequence of the fact that the charge used to store a bit decreases with each new generation, whereas the ion track remains constant. In spite of this, the numbers are reassuring. Only in some conditions does the neutron threat appear to be of some significance, but nowhere large enough to defy current mandatory ECC requirements.

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