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Test of ATLAS RPCs Front-End electronics

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Abstract

The Front-End Electronics performing the ATLAS RPCs readout is a full custom 8 channels GaAs circuit, which integrates in a single die both the analog and digital signal processing. The die is bonded on the Front-End board which is completely closed inside the detector Faraday cage.

About 50 000 FE boards are foreseen for the experiment. The complete functionality of the FE boards will be certificated before the detector assembly. We describe here the systematic test devoted to check the dynamic functionality of each single channel and the selection criteria applied. It measures and registers all relevant electronics parameters to build up a complete database for the experiment.

The statistical results from more than 1100 channels are presented.

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1. Introduction

The Front-End Electronics performing the ATLAS RPCs readout [1–4] is a full custom 8 channels GaAs circuit, which integrates in a single die both the analog and digital signal processing. Its function is to amplify, discriminate and convert the detector signals to ECL standard. The die is bonded on the Front-End Board which is mounted on the pickup strips panel and therefore completely closed inside the detector Faraday cage. This peculiarity avoids the use of interconnection cables that would degrade the analog signals transmitted to the FE Electronics. However, it requires to

certify the complete functionality of the FE board before the detector assembly.

2. The electronics and the experimental setup

The Electronics was conceived to guarantee good time performances with high counting rate, adequate immunity with respect to the noise and radiation hardness. The chip is based on a three stage wide band voltage amplifier and on a variable threshold comparator. The frequency response has its maximum at 100 MHz with a 3 dB bandwidth ranging from 50 to 150 MHz. The output is bipolar resulting in zero-integrated charge to avoid possible dependence of the steady output level on high counting rate. The amplifier cascade is AC coupled.

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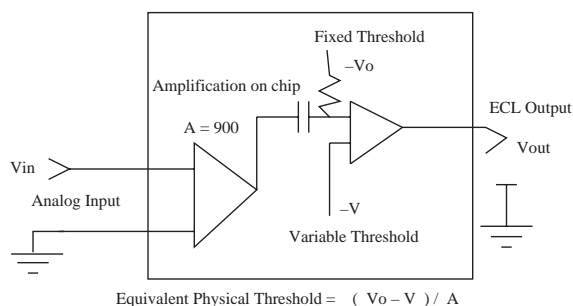


Fig. 1. A simplified sketch of FE Electronics signal processing.

A simplified scheme of the full signal processing is sketched in Fig. 1, where V_0 and V are the fixed and the variable comparator polarization voltages, respectively.

According to the production quality control procedures a DC electrical test is performed, before and after the bonding of the die on the board, by the companies interested in the production. The test is devoted to check the continuity of electrical lines, the power consumption and the voltage levels in input and output. The final AC test is performed in our laboratories to check the full dynamical functionality of all 8 channels of the board and to measure relevant electronics parameters to build up a complete database for the experiment.

The testing facility is composed of a pulse generator and a VXI-bus, equipped with a controller VXI-MXI board (interfaced with a PC) and with modules for power supplies and readout of DC voltage levels (see Fig. 2). The full system provides fast signal transmission and high-speed signal acquisition. A Bridge View software program controls each step and performs the following automatic AC test procedure.

The supplied voltage (V_{cc}), the fixed voltage threshold on comparator (V_0), the currents at each analog and digital stage (I_a, I_b, I_c, I_d) are measured, together with the environment temperature (T).

A fixed input signal V_{in} of 0.5 mV amplitude, 1.5 ns rise time and 5 ns FWHM, simulating the expected average signal from pickup strips, is injected in sequence into the 8 FE board inputs, by means of a probe system developed to minimize signal degradation and noise. The waveform

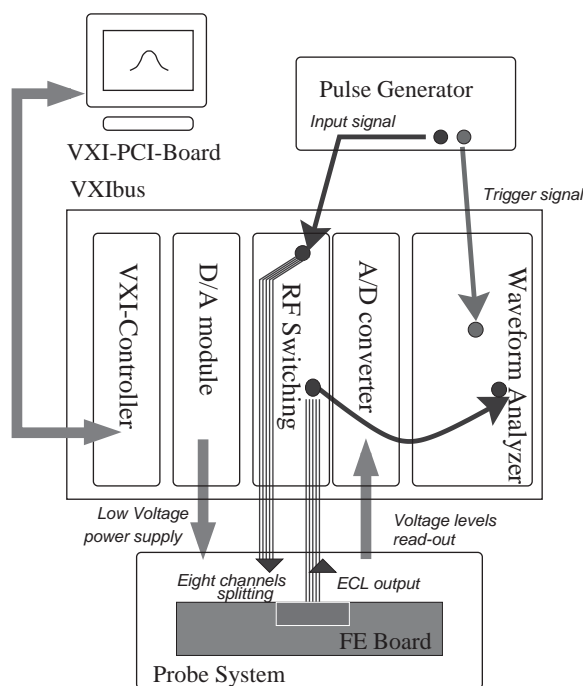


Fig. 2. The experimental setup for test is composed of a pulse generator, a personal computer, a VXIbus equipped with a controller board, a D/A module, an RF switching module, an A/D converter module and a waveform analyzer module characterized by 5 GSample/s digitizing rate and 1 GHz of analog bandwidth. The dedicated probe system was specifically developed by our working group.

analyzer module continuously monitors the output signal while the variable comparator threshold V is increased up to the value V_{switch} for which the output signal is detectable by the line receiver (at least 400 mV amplitude during more than 3 ns). The value V_{switch} , which is measured for each channel, depends on the overall analog amplification. All features of the output signal for $V = V_{switch}$ are registered together with the value of $V = V_{noise}$ which causes electromagnetic noise sensitivity.

A window of acceptable V_{switch} values is fixed around the mean of the distribution. FE boards showing at least one channel with no output signal or with V_{switch} outside of the fixed accepted window are discarded.

We present here data relative to two different FE boards samples: 1400 boards produced before

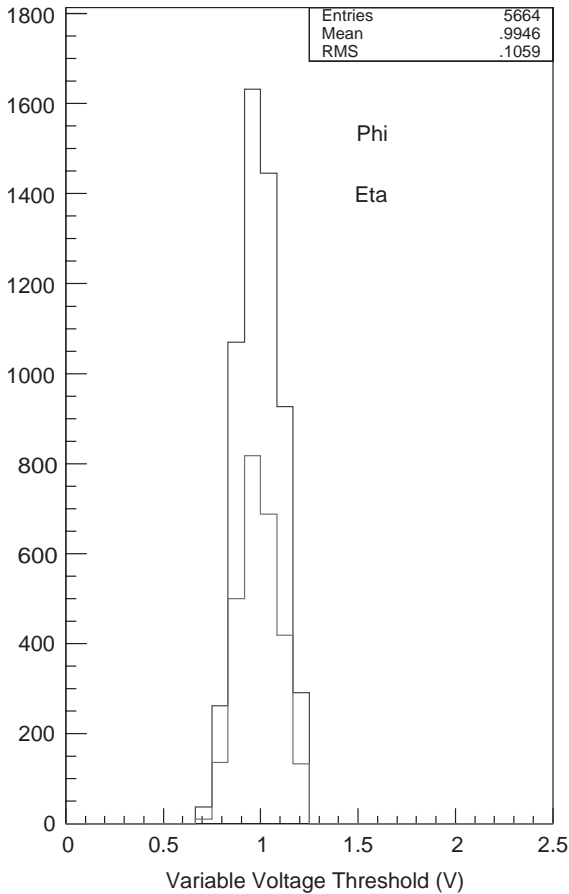


Fig. 3. The V_{switch} distribution for η and ϕ views.

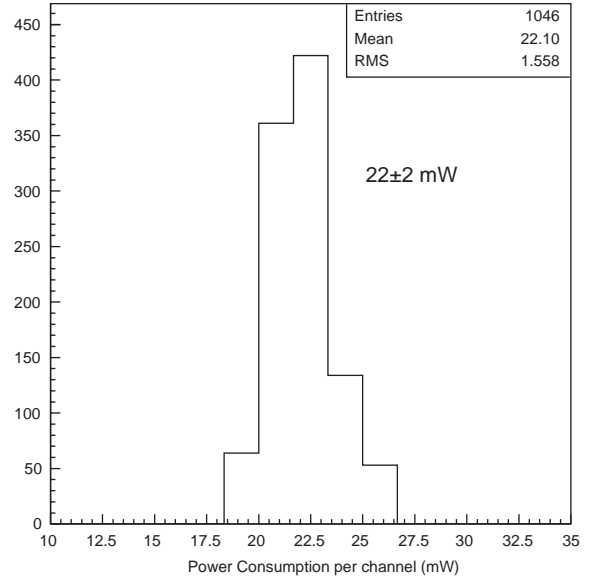


Fig. 4. Channel power consumption distribution.

the production tender (sample 1) and the first 147 boards of the standard production (sample 2).

The test of the sample 1 (11 200 channels, acceptance window from 0.7 to 1.2 V), resulted in a channel failure rate of 11.7%, and in a FE board failure rate of 21.2%. It should be stressed however that this channel failure rate characteristic of the preproduction, is higher than that of the standard production.

The Atlas RPC system is based on a bidimensional readout (η and ϕ coordinates) which requires to pick up the signals on both sides of the detector, high voltage and ground side, which give opposite signal polarity. The problem of discriminating opposite polarity input signals with the same integrated circuit, is solved introducing a

transformer, printed on the FE boards, which is connected in inverting or non-inverting configuration according to the signal polarity. Identical performances are required for the two views. Fig. 3 shows the V_{switch} distributions for η and ϕ view, which are in excellent agreement. The power consumption is 22 ± 2 mW per channel according to the distribution reported in Fig. 4.

The V_{switch} distribution of the sample 2, consisting of 1176 good functionality channels with no acceptance cut applied, is shown in Fig. 5. The effective discrimination threshold depends on the selected polarization voltage V . For example at $V = 1.15$ V (the peak of distribution), the average physical threshold on the FE electronics is 0.5 mV, i.e. the amplitude of the test input signal. The corresponding prompt charge threshold, if the input signal time profile is taken into account, is 0.09 ± 0.03 pC. Comparison of the charge threshold with the RPC prompt charge distribution [5], relative to the Atlas gas mixture, shows that the efficiency loss due to the FE electronics would be $\leq 5 \times 10^{-3}$ for a proper choice of the working voltage. The distribution of time delay with no systematic corrections applied is shown in Fig. 6 for all channels. The corresponding standard

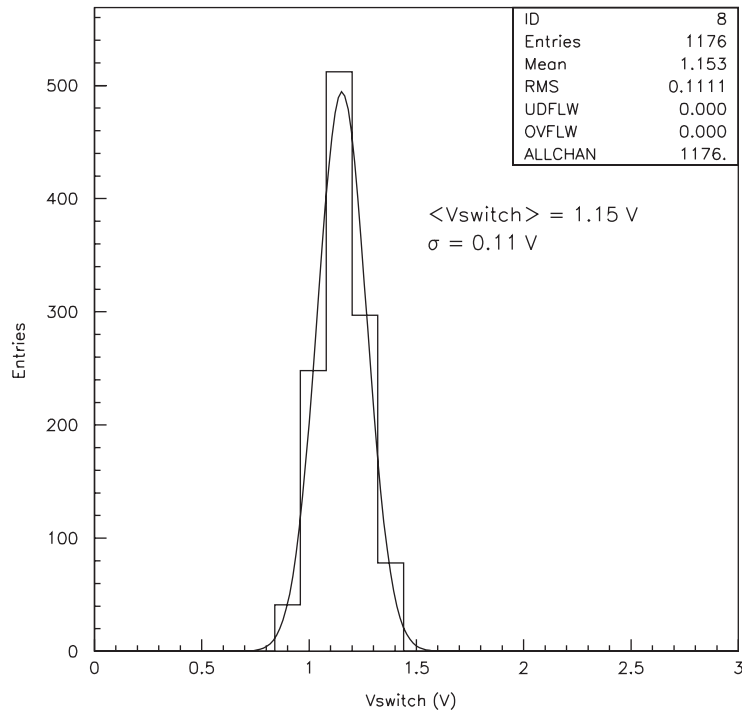


Fig. 5. The V_{switch} distribution.

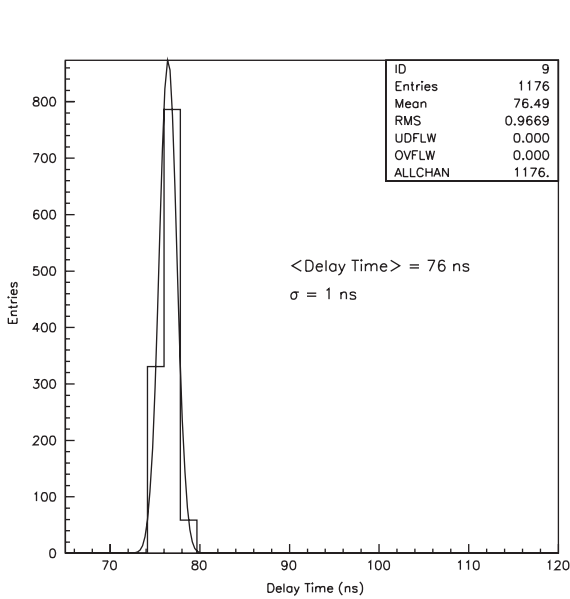


Fig. 6. The delay time distribution.

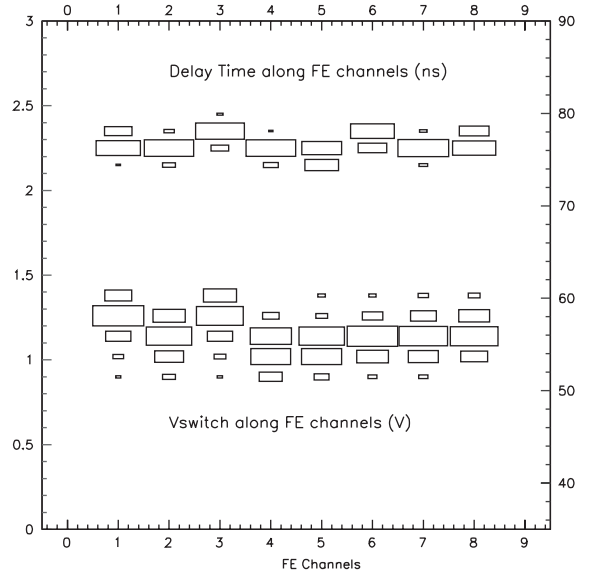


Fig. 7. The V_{switch} (in V, on left scale) and delay time (in ns, on right scale) versus FE channels.

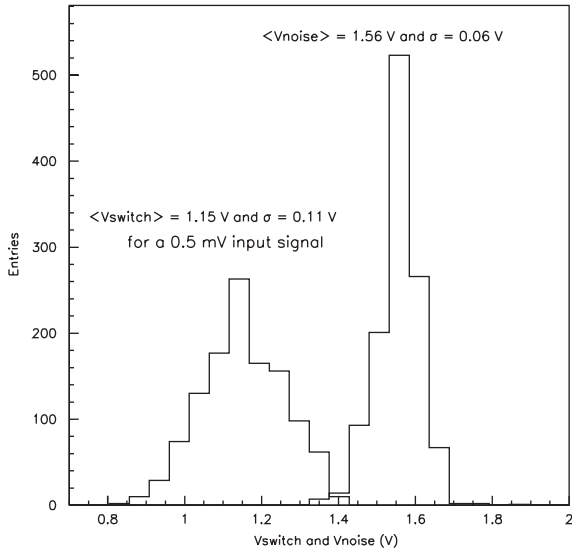


Fig. 8. The V_{switch} and the V_{noise} distributions.

deviation is less than 1 ns. With the purpose of studying the channel uniformity inside the circuit we report in Fig. 7 the distributions of V_{switch} and

of the time delay versus the chip channel number (ranging from 1 to 8). The distribution of minimum voltage threshold settable before noise pickup is shown in Fig. 8 and results well separated with respect to the V_{switch} distribution.

References

- [1] R. Cardarelli, S. Ciorciolini, V. Chiostrì, G. Orengo, An 8-channels GaAs IC front-end discriminator for RPC particle detectors, GAAS 98 Conference, Amsterdam, 1998.
- [2] G. Orengo, R. Cardarelli, S. Ciorciolini, E. Johansen, Multichannels GaAs MMIC front-end gas chamber particle detectors, GAAS 97-European Gallium Arsenide and related III-V compounds Application Symposium, Bologna, Italy, 1997.
- [3] R. Cardarelli, S. Ciorciolini, V. Chiostrì, G. Orengo, 8-channels GaAs IC front-end discriminator for RPC particle detectors, IV International Workshop on Resistive Plate Chamber and Related Detectors, Napoli, Italy, 1997.
- [4] G. Aielli, et al., Nucl. Instr. and Meth. A 409 (1998) 291.
- [5] P. Camarri, et al., Nucl. Instr. and Meth. A 414 (1998) 317.