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RESEARCH ARTICLE

Three-State Matching Technique for Designing Large Back-Off Doherty Power Amplifier

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ABSTRACT This paper presents a systematic design methodology for asymmetric Doherty power amplifiers (ADPAs) that explicitly considers multiple operational regions in the design of output matching networks. To enhance efficiency in the output back-off (OBO) region, the proposed approach employs Three-State Matching (TSM), in which the load-modulated impedance of the main amplifier is transformed into the transistor's optimal impedance at three distinct operating points. The method further incorporates an optimization process based on the optimal region (OR), where the input impedance trajectory of the matching networks is confined within the region identified by load-pull and source-pull simulations. To extend bandwidth, a post-matching network is employed to achieve robust impedance transformation. To validate the proposed technique, an ADPA utilizing 10 W and 30 W GaN HEMT devices was designed and fabricated for the n78 band (3.3–3.8 GHz) of 5G systems. Continuous-wave (CW) measurements confirm an OBO region of 9.5 dB with drain efficiency exceeding 45% across the target bandwidth. The results demonstrate that the proposed TSM-based design methodology effectively addresses efficiency degradation in the OBO region while ensuring wideband operation for next-generation wireless communication systems.

INDEX TERMS Asymmetrical doherty power amplifier, output power back-off, three states matching, efficiency, optimal region.

I. INTRODUCTION

The escalating demand for high-speed and high-capacity data transmission is a defining characteristic of modern wireless communication. Meeting this demand is driving the expansion of system bandwidths and the adoption of advanced digital modulation techniques. However, these techniques inherently result in transmitted signals with a high Peak-to-Average Power Ratio (PAPR). Under such high-PAPR conditions, traditional power amplifiers (PAs)—which are the largest energy consumers in a communication system—suffer from significant efficiency deterioration at low power levels. Resolving this critical issue is essential for the energy efficiency and operational cost of modern wireless infrastructure.

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To mitigate the efficiency challenges posed by high-PAPR signals, various PA topologies have been developed. Among them, the Doherty Power Amplifier (DPA) [1], [2], [3] is one of the most widely adopted architectures, particularly in sub-6 GHz cellular base stations. The DPA operates based on the principle of load modulation, where the load impedance presented to the active devices changes as a function of the input power level. A conventional DPA comprises a main PA (typically Class AB) and an auxiliary PA (typically Class C) of equal size, which enables an output power back-off (OBO) of approximately 6 dB while maintaining high efficiency.

However, modern communication standards generate signals with PAPRs frequently exceeding 6 dB, which conventional DPA designs struggle to handle efficiently. Consequently, significant research has focused on extending the OBO range and the high-efficiency region. Solutions

include multi-way, multi-stage, and DPA-like topologies [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. While multi-stage and multi-way DPAs feature multiple devices and offer several points of peak efficiency to extend the OBO, they often suffer from limited bandwidth and increased circuit complexity. The two-way asymmetric DPA, which uses two transistors with the auxiliary device being larger than the main, is often preferred due to its simpler structure and compact size.

The design process of a DPA effectively starts by carefully determining the dimensions of the main and auxiliary transistors. This critical step is predicated on the required peak power levels and the desired OBO to ensure optimal performance and efficiency. The auxiliary PA is designed to operate optimally at peak power (saturation). Following this, the main PA is optimized for performance at two power levels: (1) at peak power, where both transistors are saturated, and (2) at the power level where the auxiliary PA begins to turn on. This technique is known as two-state matching [26], [27].

Fig. 1(a) illustrates the typical efficiency profile of a conventional DPA as a function of output power. As shown, high efficiency is achieved at the onset of the Doherty region—corresponding to the point where the auxiliary PA begins to turn on (referred to in this paper as the low-power (LP) state)—and again at peak power (PP), where both PAs operate in saturation. However, the efficiency degrades in the intermediate OBO region. This degradation becomes more pronounced as the separation between the LP and PP states increases, i.e., as the targeted OBO level becomes larger.

A review of the existing literature on asymmetric DPAs indicates that the mid-region of the Doherty operation—namely, the power interval between auxiliary turn-on and full saturation—has not been systematically incorporated into the impedance optimization process. Most reported designs focus primarily on the two end states of load modulation, i.e., the auxiliary turn-on point and the peak-power condition. In [28], efficiency degradation in the intermediate Doherty region was addressed for a symmetric DPA with 6 dB OBO by compensating for the phase variation of the peaking amplifier using an offset line, and the solution was demonstrated at a single frequency. However, a generalized impedance-synthesis approach that explicitly targets intermediate power levels, particularly for asymmetric DPAs with large OBO and broadband operation, has not been fully developed. Moreover, optimizing an asymmetric DPA over the entire OBO range and across a wide frequency band typically requires extensive harmonic-balance analysis involving two nonlinear active devices. This significantly increases computational complexity and may hinder the convergence of computer-aided optimization routines.

This paper introduces a systematic and novel design methodology for asymmetric DPAs with extended output power back-off (OBO). Unlike conventional two-state approaches, the proposed design employs a Three-State

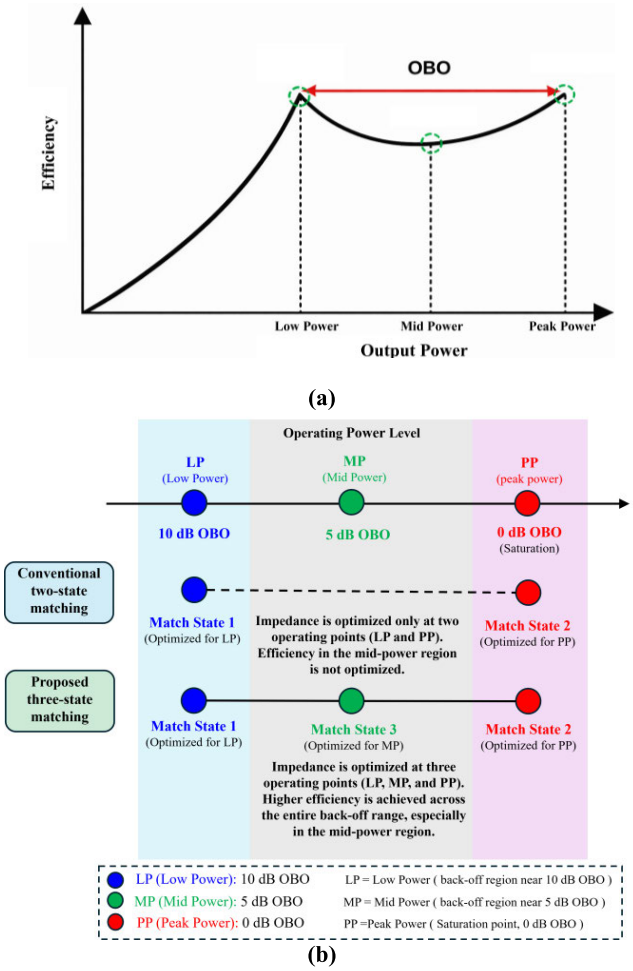

FIGURE 1. (a) Efficiency vs. output power of a typical DPA, (b) Definition of the low-power (LP), middle-power (MP), and peak-power (PP) operating states used in the proposed three-state matching (TSM) technique.

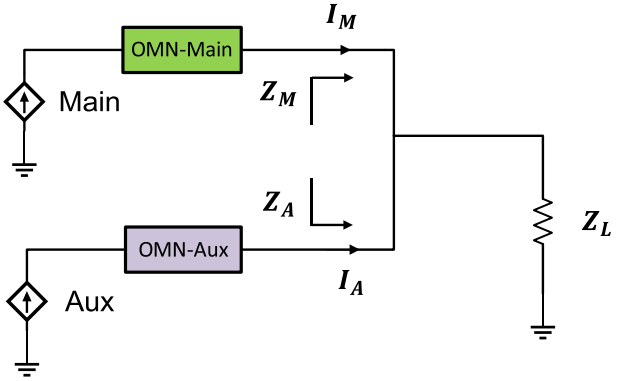

FIGURE 2. Simplified operational diagram of a conventional DPA.

Matching (TSM) technique, which considers three distinct operating conditions for the synthesis of the main amplifier output matching network:

- PP state: Both devices are in saturation.

- LP state (turn-on state): The auxiliary device is just beginning to turn on.
- Middle power (MP) state: An additional operating point located near the center of the Doherty back-off region.

By incorporating the MP state into the matching-network synthesis, the proposed TSM approach effectively mitigates the efficiency degradation commonly observed in the middle of the Doherty operating region. The TSM technique enables impedance optimization at three operating power levels, resulting in more accurate impedance control across a wider output-power range while preserving the simple and compact structure of a conventional asymmetric DPA.

As illustrated in FIGURE 1(b), the main contribution of this work is the introduction of the MP operating point as an additional design constraint in the synthesis of the main-path output matching network. In contrast to conventional approaches that rely solely on low-power and peak-power operating conditions, the proposed method explicitly incorporates the MP operating state, thereby enabling more accurate load-modulation-based impedance synthesis and improved efficiency throughout the Doherty operating region.

To achieve a wide bandwidth, we employ a transformer-less load-modulated DPA configuration where the impedance converter is embedded within the output-matching network [26]. In conventional DPAs, load modulation between the main and auxiliary amplifiers is typically realized using a quarter-wavelength (λ /4) transmission line [29]. However, the inherent frequency-dependent characteristics of the λ /4 transformer limit the achievable bandwidth, as discussed in [29]. To overcome this limitation, transformer-less load-modulation techniques have been introduced, which eliminate the frequency-sensitive impedance transformation of the λ /4 network and enable broadband operation [26]. Therefore, a transformer-less architecture is adopted in this work to enhance the operational bandwidth while preserving effective load modulation and high-efficiency performance. An additional post-matching network is utilized to transform the 50 Ω output impedance to a suitable impedance at the common output node [30], [31], [32], [33], [34]. Moreover, the input and output matching networks are strategically designed to confine the impedance trajectory within the Optimal Region (OR), which is identified via load-pull and source-pull simulations [35], [36], [37], [38], [39], [40].

To validate the TSM-based design, an asymmetric DPA utilizing 10 W and 30 W GaN HEMT devices was designed and fabricated for the 3.3–3.8 GHz band, targeting sub-6 GHz 5G communications. Continuous-wave (CW) measurements confirm an OBO greater than 9.5 dB with high efficiency across the target bandwidth.

The remainder of this paper is organized as follows: Section II details the novel asymmetric Doherty design technique based on Three-State Matching. Section III describes the complete amplifier design process. Section IV presents the measured results and the performance of the fabricated prototype, followed by the Conclusion.

II. METHOD OF THREE-STATE MATCHING

FIGURE 2 illustrates a simplified model of a DPA, consisting of a main and an auxiliary PA branch modeled as ideal current sources with output matching networks. The equivalent load-modulated impedances seen by the main and auxiliary transistors at the common output node are denoted by Z_M and Z_A, respectively, and are obtained as follows [3]:

$$\mathbf{Z_M} = \left(1 + \frac{\mathbf{I_A}}{\mathbf{I_M}}\right) Z_L \tag{1}$$

$$\mathbf{Z_A} = \left(1 + \frac{\mathbf{I_M}}{\mathbf{I_A}}\right) Z_L \tag{2}$$

$\mathbf{I_M}$ and $\mathbf{I_A}$ are the complex output currents injected by the two branches (see FIGURE 2), and Z_L represents the load impedance at the combining node.

In the proposed design methodology of DPA, the design steps are as follows:

1. According to the desired specifications (peak power, OBO value), the transistors and the operating points of the main and auxiliary amplifiers are selected.

2. The auxiliary amplifier is designed for optimal performance at the PP state. This step is exactly the same as in the conventional DPA design method.

3. Considering the effect of the auxiliary amplifier, the main amplifier's output matching network is designed to achieve optimal performance across the three required states: LP, MP, and PP. This is the key step distinguishing between our work and the conventional design of DPA, where a two-state matching network design is applied.

In step 2, the load modulated impedances seen by the auxiliary device at the PP condition are needed. Moreover, step 3 requires the modulated impedances seen by the main device at the three power level conditions, LP, MP, and PP. Therefore, in the following subsection, we first analyze the modulated impedances seen by each device at these power levels. Then in subsection B, we will talk about the design of the matching network of the main device using the proposed TSM technique.

A. ANALYSIS OF MODULATED IMPEDANCES AT THREE POWER STATES

1) LOW POWER STATE

In the LP state, the auxiliary device is intentionally off (or just beginning to turn on). Consequently, the auxiliary amplifier's output presents a reactive component, *jX(f)*, at the common node (FIGURE 3(a)). This reactive component is in parallel with the load impedance Z_L and determines the load impedance $\mathbf{Z_M^{LP}}$ seen by the main amplifier.

2) PEAK POWER STATE

At the PP state, both the main and auxiliary transistors operate in saturation. To achieve maximum power in the PP state, the currents $\mathbf{I_M}$ and $\mathbf{I_A}$ must be in phase, i.e., $\angle\mathbf{I_M^{PP}} = \angle\mathbf{I_A^{PP}}$ (superscripts denote the working power condition). This phase alignment is achieved by applying an appropriate offset

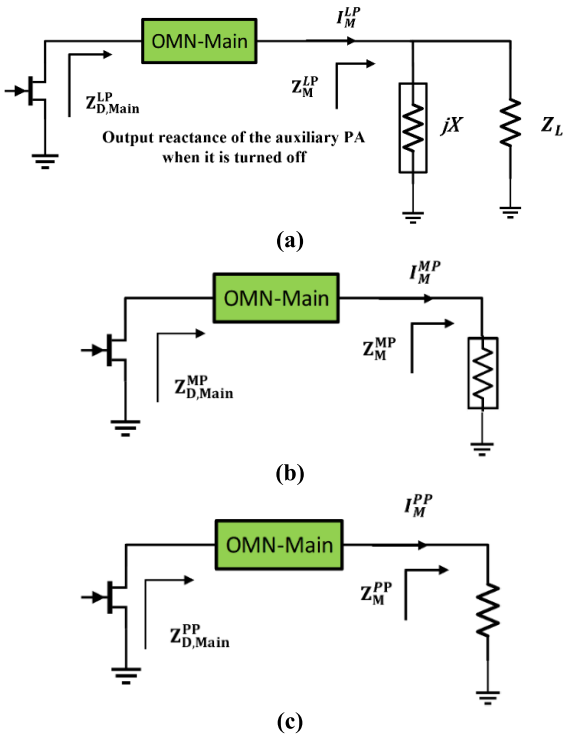

FIGURE 3. Simplified schematic of the main amplifier's output section at three power states: (a) low power, (b) intermediate power, and (c) peak power.

in the input/output of the auxiliary PA branch. The current magnitude ratio at PP is defined as $R_I^{PP} = |\mathbf{I_A^{PP}}|/|\mathbf{I_M^{PP}}|$. which is determined during the initial design stage based on the required peak power and each branch's power contribution. Under the in-phase condition, the modulated load impedances given in (1) and (2) can be derived as follows [3]:

$$Z_M^{PP} = \left(1 + R_I^{PP}\right) Z_L \tag{3}$$

$$Z_A^{PP} = \left(1 + \frac{1}{R_I^{PP}}\right) Z_L \tag{4}$$

3) MIDDLE POWER STATE

The MP operating point is defined as the midpoint of the target OBO region, as shown in FIGURE 1(b). For instance, for a Doherty amplifier designed with a target OBO of 10 dB, the MP operating point is selected at 5 dB OBO. In the MP state, both the main and auxiliary transistors are active; the main transistor remains in saturation, while the auxiliary transistor is active but has not yet reached saturation. Assuming the output currents' magnitude ratio $R_I^{MP} = |\mathbf{I_A^{MP}}|/|\mathbf{I_M^{MP}}|$ and phase difference $\Delta\theta^{MP} = \angle\mathbf{I_A^{MP}} - \angle\mathbf{I_M^{MP}}$, we obtain that the impedances seen at the output, $\mathbf{Z_M^{MP}}$ and $\mathbf{Z_A^{MP}}$ can be derived from (1) and (2) as follows:

$$\mathbf{Z_M^{MP}} = \left(1 + R_I^{MP} \exp\left\{j\Delta\theta^{MP}\right\}\right) Z_L \tag{5}$$

$$\mathbf{Z_A^{MP}} = \left(1 + \frac{1}{R_I^{MP}} \exp\left\{-j\Delta\theta^{MP}\right\}\right) Z_L \tag{6}$$

As mentioned before, in the proposed three-state matching technique (in step 3), $\mathbf{Z_M^{MP}}$ is required. This impedance, as observed in (5), is a function of R_I^{MP} and $\Delta\theta^{MP}$. The current magnitude ratio $R_I^{MP} = |\mathbf{I_A^{MP}}|/|\mathbf{I_M^{MP}}|$ can be approximately obtained from the ratio of power delivered by each device at the MP state. The phase difference $\Delta\theta^{MP} = \angle\mathbf{I_A^{MP}}$ - $\angle\mathbf{I_M^{MP}}$ is unknown at this stage of the design (step 3), because the phase of the main amplifier's output current ($\angle\mathbf{I_M^{MP}}$) depends on its output matching network, which is currently under design and not yet determined.

To obtain $\Delta\theta^{MP}$, we use the following strategy. Since the main amplifier remains in saturation throughout the Doherty region, its output voltage is nearly constant. This means the output capacitance and the resulting output phase of the main transistor are largely stable, leading to an approximation of constant phase for the main current: $\angle\mathbf{I_M^{MP}} \approx \angle\mathbf{I_M^{PP}}$ [3]. Considering the in-phase condition at peak power ($\angle\mathbf{I_A^{PP}} = \angle\mathbf{I_M^{PP}}$), the phase difference $\Delta\theta^{MP} = \angle\mathbf{I_A^{MP}}$ - $\angle\mathbf{I_M^{MP}}$ can be expressed as follows:

$$\Delta\theta^{MP} \approx \angle\mathbf{I_A^{MP}} - \angle\mathbf{I_A^{PP}} \tag{7}$$

As observed from (7), determining the phase difference $\Delta\theta^{MP}$ requires knowledge of the auxiliary current phase in the MP and PP states (notice that, unlike the MN of the main device, which is not designed during step 3, the MN of the auxiliary device is already determined in step 2). These mandates simulate the auxiliary PA when terminated by the modulated loads $\mathbf{Z_A^{MP}}$ and $\mathbf{Z_A^{PP}}$. However, while $\mathbf{Z_A^{PP}}$ is calculated and known from (4), the impedance, $\mathbf{Z_A^{MP}}$ itself, is a function of the unknown phase difference $\Delta\theta^{MP}$ (as shown in (7)). This establishes a complex, interdependent relationship that cannot be solved explicitly. To extract $\Delta\theta^{MP}$ an iterative algorithm is employed as follows:

1. An initial estimate of $\Delta\theta^{MP}$ is selected.
2. The corresponding value of $\mathbf{Z_A^{MP}}$ is calculated using (6).
3. The auxiliary amplifier is terminated with $\mathbf{Z_A^{MP}}$ and the output current phase at the MP is then simulated, yielding the phase $\angle\mathbf{I_A^{MP}}$
4. The auxiliary amplifier is terminated with $\mathbf{Z_A^{PP}}$ and the output current phase at the PP is then simulated, yielding the phase $\angle\mathbf{I_A^{PP}}$.
5. The phase difference is updated according to $\Delta\theta^{MP} = \angle\mathbf{I_A^{MP}}$ - $\angle\mathbf{I_A^{PP}}$
6. A new value of $\mathbf{Z_A^{MP}}$ is recalculated based on the updated phase difference.
7. The updated $\mathbf{Z_A^{MP}}$ is again applied as the modulated load impedance at the MP. The phase $\angle\mathbf{I_A^{MP}}$ is recalculated, followed by an updated evaluation of $\Delta\theta^{MP} = \angle\mathbf{I_A^{MP}}$ - $\angle\mathbf{I_A^{PP}}$
8. Steps 2 to 7 are repeated iteratively until $\Delta\theta^{MP}$ converges to a stable value.

Once $\Delta\theta^{MP}$ is determined, $\mathbf{Z_M^{MP}}$ which is required in step 3 of the TSM technique, can be calculated using (5).

B. OUTPUT MATCHING NETWORK DESIGN USING TSM

In the TSM method, the MN is designed to match three sets of impedances (at three states: LP, MP and PP) to each other as shown in FIGURE 3. In this figure, the impedance seen from the right side of the OMN of the main device is $\mathbf{Z_M^{LP}}$, $\mathbf{Z_M^{MP}}$, and $\mathbf{Z_M^{PP}}$. These impedances are to be matched to the optimum impedances that the drain of the main device needs to see at three states, $\mathbf{Z_{D,Main}^{LP}}$, $\mathbf{Z_{D,Main}^{MP}}$, and $\mathbf{Z_{D,Main}^{PP}}$ which can be determined using the load-pull simulation of the main device at three states. This method is described in detail in a design example given in the next section.

III. DESIGN EXAMPLE

To validate the TSM methodology proposed in Section II, an ADPA was designed using GaN High-Electron-Mobility Transistors (HEMTs). The circuit targets the 5G n78 frequency band (3.3–3.8 GHz). The primary design goals were to achieve a peak output power ($Pout_{peak}$) of 46 dBm (40 W) and maintain a drain efficiency (DE) greater than 50% from a 10-dB OBO level up to saturation.

To meet the specified design requirements, the Wolfspeed GaN HEMT devices CGH40010F and CGHV40030F are selected for the main and auxiliary amplifier paths, respectively. The main device is biased in Class-AB operation with $V_{DS} = 28$ V and $V_{GS} = -2.95$ ($I_{DQ} = 100$ mA). In contrast, the auxiliary transistor is biased in Class-C with $V_{DS} = 50$ V and $V_{GS} = -4.6$ V. The use of a high-voltage (50 V) transistor for the auxiliary stage is employed to compensate for the lower inherent gain of Class-C operation relative to the 28 V Class-AB main stage.

At the peak output power of 40 W, the auxiliary amplifier contributes around 30 W, and the main amplifier delivers 10W. The power ratio was selected based on the target specifications of 40-W peak output power and 10-dB OBO in the proposed asymmetric Doherty amplifier [3], rather than through comparative optimization of different power-ratio configurations. Given the voltage ratio $V_{D,A}/V_{D,M} \approx 1.8$, the corresponding current ratio at PP state ($R_I^{PP} = |\mathbf{I_A^{PP}}|/|\mathbf{I_M^{PP}}|$) is determined to be approximately 1.66.

By performing load-pull simulations for both devices, we found that the optimal drain impedances for achieving maximum performance within our frequency band of interest are significantly lower than 50 Ω, typically in the range of 5–10 Ω. Therefore, to simplify the design of the output matching networks (OMNs), the load impedance is set to $Z_L = 5\Omega$ in FIGURE 2. It should be noted that this choice — rather than adopting the standard 50 Ω load—facilitates the OMN design. However, a post-matching network is required at the output to transform 5 Ω to 50 Ω.

Load-pull simulations were performed in Keysight ADS using the nonlinear compact models of the devices from Wolfspeed under harmonic-balance analysis. Five harmonics were included in the simulations. The second harmonic was explicitly incorporated into the optimization process, while the third to fifth harmonics were terminated under open-circuit conditions. The built-in device thermal model was employed throughout the simulations. The load-pull analysis was carried out over the 3.2–3.9 GHz frequency range with a frequency step of 0.1 GHz. To ensure numerical accuracy, the ADS strict convergence option was used, corresponding to a relative error below 10^{-4} and an output-power variation of less than 0.01 dB between successive iterations.

A. AUXILIARY AMPLIFIER DESIGN

The auxiliary amplifier is designed to achieve maximum output power and efficiency at the PP level, where the device operates in saturation. Based on (4), and with the determined current ratio $R_I^{PP} = 1.66$ and $Z_L = 5\Omega$, the impedance observed by the auxiliary amplifier at the common output node under the PP state is calculated to be approximately 8 Ω.

For the auxiliary amplifier design, the optimum transistor drain impedances across the target frequency band are determined using the load-pull technique. Power added efficiency (PAE) and output power contours are obtained at several frequency points. The fundamental load impedance region is defined by the intersection of the PAE≥70% contour and the Pout≥45 dBm contour, as shown in FIGURE 4(a).

On the other hand, transistor terminations at higher-order harmonics, particularly the second harmonic, affect the performance of the PA [41], [42], [43]. In this work, only the impact of the second harmonic is considered, as it has the most dominant influence. FIGURE 4(b) illustrates the DE variation with respect to the phase of the second-harmonic reflection coefficient ($\angle\Gamma(2f)$). A considerable degradation in DE is observed for termination phases in the range of −150° to −110°, which is consequently identified as the undesirable region to be avoided.

To mathematically define the target regions, load-pull simulations are first performed to obtain the output-power and PAE contours at each design frequency. Based on the selected performance targets, the overlap of the corresponding contours defines the desired high-performance impedance region. Since this overlap generally has an irregular shape, it is approximated by circle-based boundaries to facilitate matching-network optimization. The centers and radii of these circles are extracted using the ADS optimization and curve-fitting tools, following the optimal-region methodology reported in [35] and [38]. The optimal region (OR) for the fundamental impedance is then formulated as the intersection of these two circles as follows [38]:

$$\begin{aligned} |\,\mathbf{\Gamma}(f_i) - \mathbf{C_P}(f_i)\,| &\le R_P(f_i) \\ |\,\mathbf{\Gamma}(f_i) - \mathbf{C_E}(f_i)\,| &\le R_E(f_i) \end{aligned} \tag{8}$$

The optimal region for the second-harmonic termination is defined by excluding the undesirable phase range around the Smith chart as follows [38]:

$$\begin{aligned} &|\,\mathbf{\Gamma}(2f_i)\,| \ge 0.9 \\ &\angle\mathbf{\Gamma}(2f_i) \notin [-150; -110] \end{aligned} \tag{9}$$

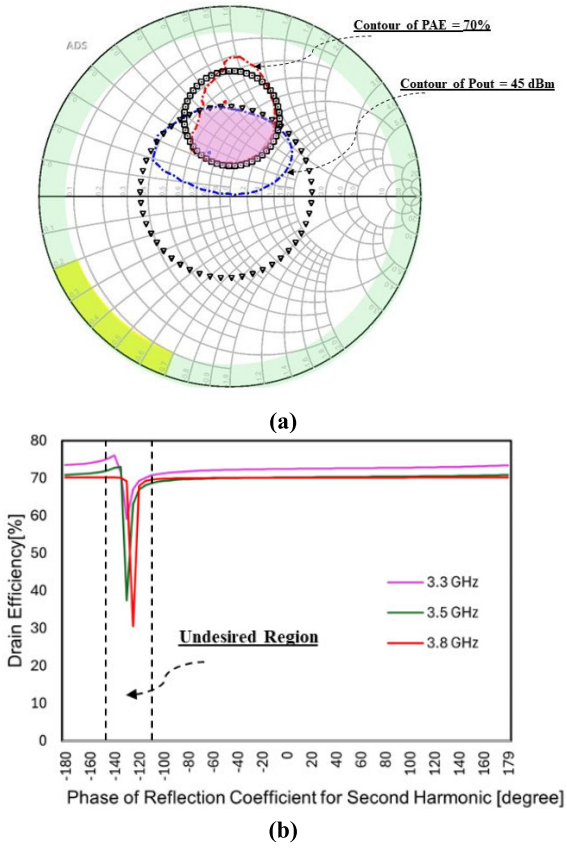

FIGURE 4. (a) The selected PAE and Pout contours (PAE = 70% and Pout = 45dBm) define a common region (pink region), which can be approximated using arcs from two circles. A portion of the allowed region for the second harmonic termination is also shown in green shade. (b) DE versus the phase of Γ at second harmonic (its magnitude is fixed at 0.9) for the auxiliary device.

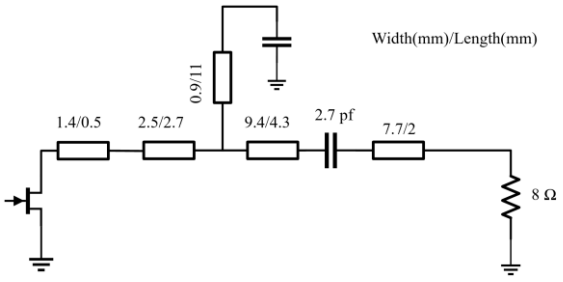

FIGURE 5. The schematic of the designed OMN of the auxiliary PA.

In (8) and (9), f_i denotes a frequency point within the desired operating band, and $\Gamma(f_i)$ denotes the input reflection coefficient of the matching network at f_i. $\mathbf{C_P}$ and R_P are the center and radius of the circle associated with the output power contour, and $\mathbf{C_E}$ and R_E are for the PAE contour. The centers and radii used to define the ORs are summarized in TABLE 1.

The OMN was synthesized as a multi-section transmission line network, incorporating a high-impedance stub for DC biasing (FIGURE 5). The lengths and widths of the transmission lines were determined using the built-in optimizer in

TABLE 1. The centers and radii of the OR of the auxiliary amplifier.

f(GHz)	$\mathbf{C_P}$	R_P	$\mathbf{C_E}$	R_E
3.2	0.0+j0.04	0.47	0.1+j0.44	0.24
3.3	-0.0+j0.05	0.45	0.08+j0.43	0.23
3.4	-0.03-j0.0	0.48	-0.0+j0.42	0.25
3.5	-0.06-j0.01	0.46	-0.04+j0.37	0.25
3.6	-0.10-j0.04	0.46	-0.1+j0.35	0.26
3.7	-0.10-j0.06	0.45	-0.15+j0.33	0.27
3.8	-0.10-j0.06	0.45	-0.12+j0.38	0.25
3.9	-0.10-j0.06	0.45	-0.15+j0.33	0.27

TABLE 2. The centers and radii of the or of the main amplifier at three states: (A) LP, (B) MP, AND (C) PP.

(a)

f(GHz)	$\mathbf{C_E}^{\mathbf{LP}}$	R_E^{LP}
3.2	0.09+j0.36	0.47
3.3	0.09+j0.26	0.43
3.4	0.09+j0.26	0.43
3.5	0.04+j0.2	0.41
3.6	0.12+j0.23	0.42
3.7	0.10+j0.24	0.43
3.8	0.12+j0.24	0.43
3.9	0.1+j0.23	0.44

(b)

f(GHz)	$\mathbf{C_E}^{\mathbf{MP}}$	R_E^{MP}
3.2	0.15+j0.27	0.47
3.3	0.2+j0.29	0.48
3.4	0.15+j0.25	0.48
3.5	0.15+j0.25	0.44
3.6	0.36+j0.27	0.36
3.7	0.0+j0.25	0.49
3.8	0.0+j0.18	0.49
3.9	0.0+j0.18	0.51

(c)

f(GHz)	$\mathbf{C_P}^{\mathbf{PP}}$	R_P^{PP}	$\mathbf{C_E}^{\mathbf{PP}}$	R_E^{PP}
3.2	0.17-j0.2	0.6	0.27+j0.24	0.35
3.3	0.17-j0.22	0.58	0.2+j0.25	0.33
3.4	0.21-j0.22	0.57	0.22+j0.2	0.33
3.5	0.34-j0.22	0.54	0.25+j0.2	0.3
3.6	0.5-j0.17	0.42	0.43+j0.16	0.26
3.7	0.04-j0.22	0.47	0.01+j0.19	0.37
3.8	0.08-j0.24	0.48	0.03+j0.16	0.4
3.9	0.12-j0.27	0.49	0.02+j0.12	0.41

Advanced Design System (ADS). This optimization ensured that the input impedance path of the OMN satisfied conditions (8) and (9) across the entire 3.2–3.9 GHz band. The resulting circuit was implemented on a Rogers RO4003C substrate with a thickness of 12 mil. Figure 6 illustrates the trajectory of Γ(f) of the realized OMN, confirming that the fundamental and second-harmonic impedances are successfully confined within their respective optimal regions. The input matching network (IMN) was conventionally designed for maximum gain.

B. MAIN AMPLIFIER DESIGN

Following the design of the auxiliary amplifier, the main amplifier is developed. The core objective of this phase is to synthesize the main OMN using the proposed TSM method introduced in Section II. The OMN must transform the three

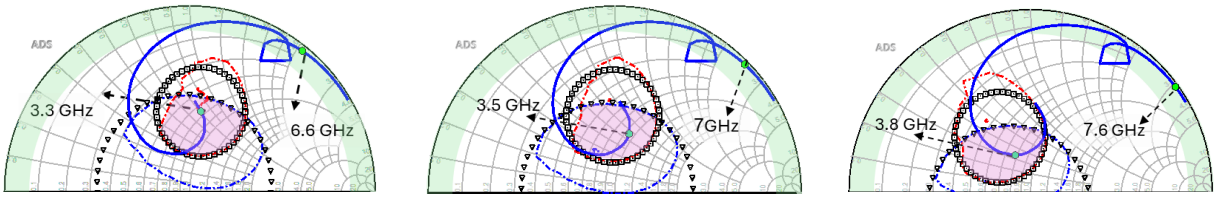

FIGURE 6. The impedance trajectory of the optimized OMN of the auxiliary PA. The optimum regions of the load at fundamental and the suitable area for the second harmonic termination are shown by pink and green shading, respectively. The contours corresponding to Pout = 45 dBm and PAE = 70% are also depicted by blue-dashed and red-dashed lines, respectively.

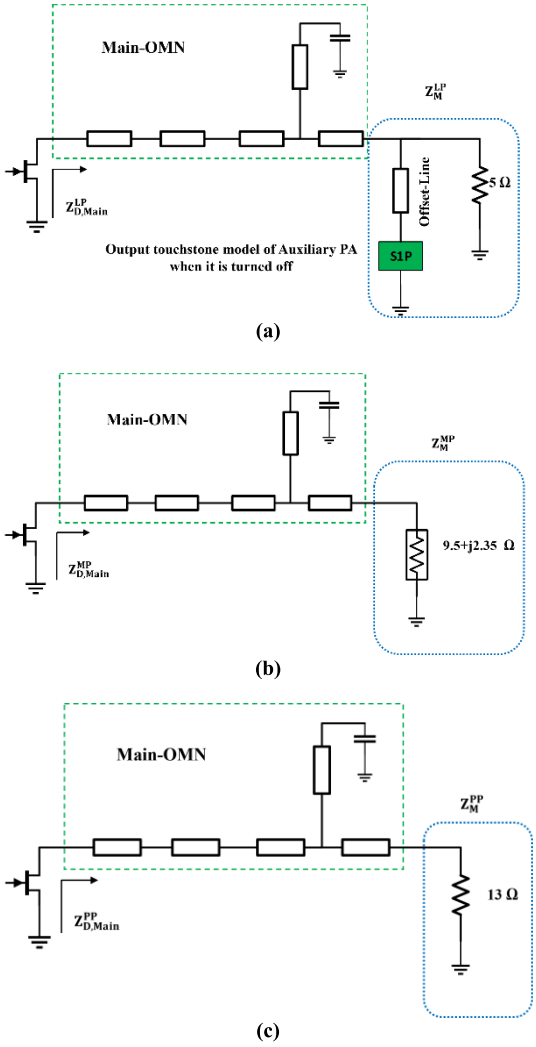

FIGURE 7. Representation of the three-state matching in the design of the output matching network of the main amplifier at low power (a), middle power (b), and peak power (c).

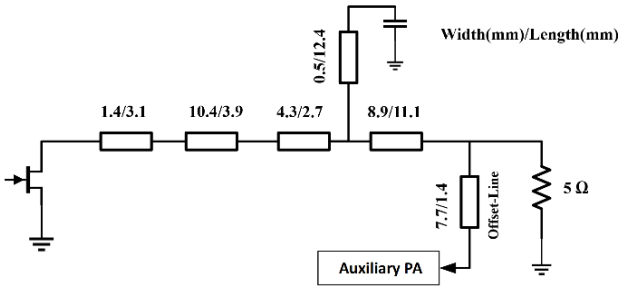

FIGURE 8. Schematic of the designed OMN for the main PA.

modulated impedances appearing at the common output node into the corresponding optimal drain impedances of the main transistor for the LP, MP, and PP states.

To achieve this, the optimal drain impedances under these three power levels are first determined. Load-pull simulations are performed to extract the PAE and Pout contours across the operating frequency band for the LP, MP, and PP states. For the LP and MP conditions, only the PAE contours are considered, while for the PP condition, the intersection of the PAE and Pout contours defines the target region.

At the LP condition (10-dB OBO) the DPA delivers approximately 36 dBm (4 W) at the system output, the bulk of which is supplied by the main amplifier. For this state the PAE contour corresponding to 50% efficiency is selected as the target region. Since the main amplifier remains saturated throughout the 10-dB back-off range (OBO $<$ 10 dB), its output power is approximately proportional to the square root of the input power (since $P_{in} \propto v_{gs}^2$ and $P_{out} \propto v_{gs}$). Therefore, in the Doherty region. We model the main amplifier output power versus input power relationship as follows:

$$\text{Pout}_{\text{Main}} = c_0 + c_1\sqrt{\text{Pin}} \tag{10}$$

Assuming a nominal power gain of around 10 dB across the 10-dB OBO range (according to the device datasheet), the input powers at the LP (10-dB OBO), MP (5-dB OBO), and PP (0-dB OBO) points are approximately 0.4 W, 1.3 W, and 4 W, respectively. Fitting the pairs (Pin, $\text{Pout}_{\text{Main}}$) = (0.4W,4W) and (4 W,10 W) into (10) gives $c_0 \approx 1.3$ and $c_1 \approx 4.3$. Using these coefficients and Pin = 1.3W for the MP state yields an estimated main-amplifier output of 6 W.

Accordingly, the PAE contour at ≈55% is chosen as the optimal region for MP. For the PP state, the optimal region is taken as the intersection of the 65% PAE contour and the 40-dBm output-power contour.

Following the identification of these regions from the load-pull contours, the corresponding target areas for the OMN design are approximated using circle-based boundaries, consistent with the optimal-region methodology adopted for the

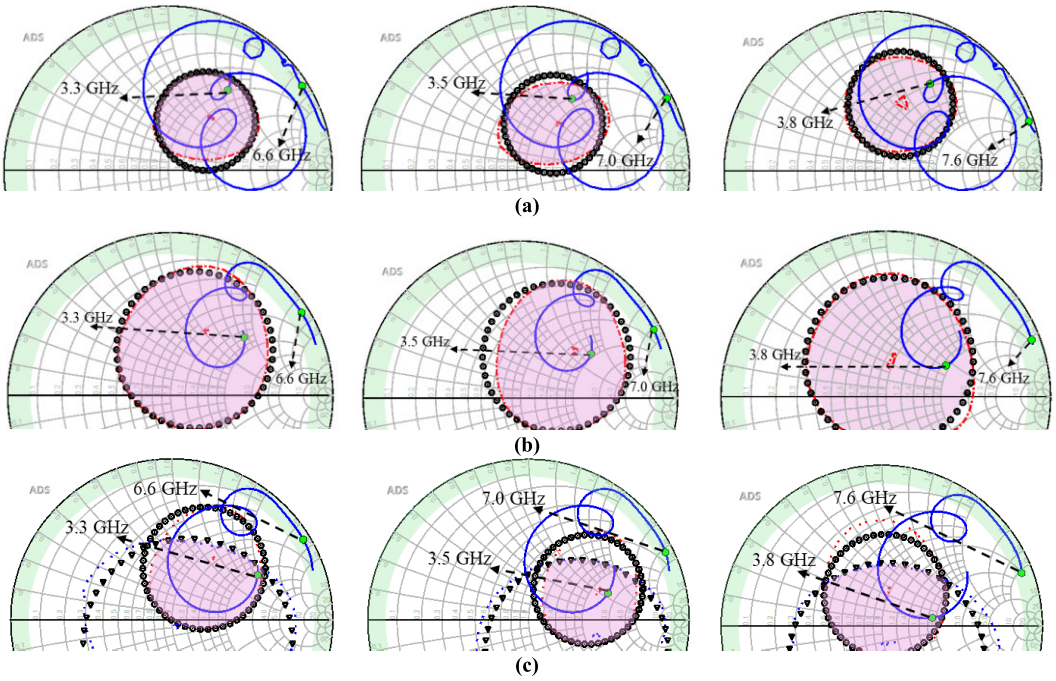

FIGURE 9. The simulated impedance trajectories for the OMN of the main PA in the (a) LP, (b) MP, (c) PP states.

auxiliary amplifier. The circle parameters are obtained using the ADS optimization tool and are subsequently used as optimization constraints for the matching-network synthesis. The centers and radii of these circles for the three operating states are listed in TABLE 2, where the subscripts ''P'' and ''E'' denote the Pout and PAE circles, respectively.

As in the auxiliary design, the influence of the second harmonic is examined. The efficiency degrades when the second-harmonic impedance phase lies between $-140°$ and $-50°$; thus, regions outside this range are adopted for OMN synthesis.

Using the analytical relations (3), (7), the noted iterative algorithm in the section II and the selected device parameters, the modulated impedances seen by the main PA at PP and MP states are calculated as 13 Ω and 9.5+j2.35 Ω, respectively, as illustrated in FIGURE 7. At the LP condition, the auxiliary path behaves as a parasitic element in the load of the main device. This parasitic loading is modeled using a one-port Touchstone (S1P) file extracted from the auxiliary amplifier output.

The main transistor's OMN, like that of the auxiliary device, consists of a multi-section transmission line structure incorporating a shunt stub that also serves as the biasing network. The ADS built-in optimizer was used to determine lengths, widths, and the offset line so that the drain impedance falls inside the optimal regions for LP, MP, and PP. The optimization targets are the three condition sets defined in (8) and (9), with circle centers and radii given in TABLE 2. The optimized circuit is shown in FIGURE 8, and the implemented OMN impedance trajectories for the three operating states are plotted in FIGURE 9; at each frequency, both the fundamental and the second harmonic lie within their respective optimum regions. Finally, the IMN was designed by conventional source-pull at the PP state to maximize power gain.

C. INTEGRATION AND FINAL TUNING OF THE ASYMMETRIC DPA

After designing the IMN and OMN for both the main and auxiliary amplifiers, the input power divider is implemented. A Gysel power divider is selected to equally split the input signal between the two amplifier branches. Compared with the conventional Wilkinson configuration [44], the Gysel topology offers superior power-handling capability due to its grounded resistive terminations and effectively mitigates parasitic effects.

At the output side, a post-matching network is incorporated to transform the 50Ω system impedance to 5Ω, ensuring proper load modulation across the Doherty operating range. The complete schematic of the designed DPA is depicted in FIGURE 10.

Following circuit integration, fine-tuning is performed to optimize the Doherty load modulation and achieve balanced operation between the main and auxiliary paths. After optimization, the drain supply voltages of the main and auxiliary transistors are set to 26V and 52V, respectively. The main transistor bias current is adjusted to 33 mA, while the gate bias voltage of the auxiliary transistor is set to -5.8V to ensure proper turn-on characteristics.

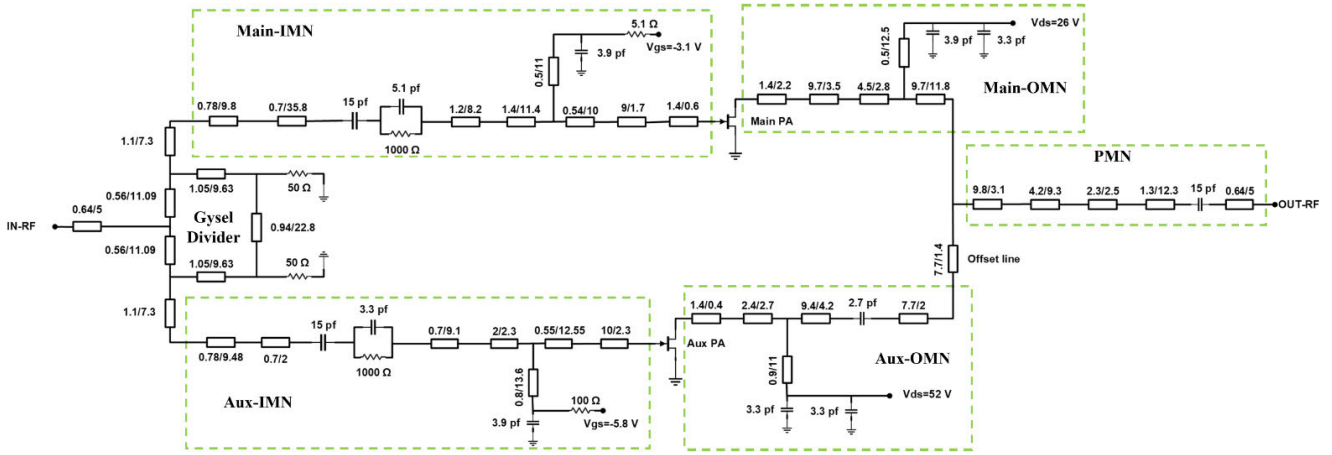

FIGURE 10. Schematic of the asymmetric DPA designed on an RO4003C substrate with a thickness of 12 mil. The transmission line dimensions (width/length) are given in millimeters.

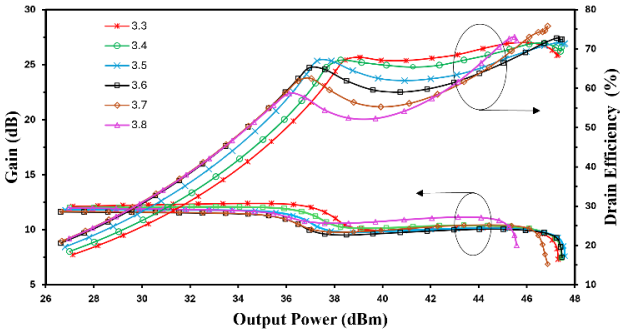

FIGURE 11. The simulated DEs and gains of the designed Asymmetric DPA versus output power.

FIGURE 11 presents the simulated DE and power gain of the full-wave electromagnetic model versus output power across the 3.3–3.8 GHz band. The results show a maximum output power between 45.7 and 47.2 dBm, with an OBO exceeding 11 dB and a DE above 50 %, confirming the effectiveness of the proposed design approach.

IV. MEASUREMENT AND EXPERIMENTAL VALIDATION

A photograph of the fabricated asymmetric DPA prototype and its measurement setup is displayed in FIGURE 12. The measured and simulated S-parameters (S_{11} and S_{21}) are compared in FIGURE 13, showing good agreement from 2 to 6 GHz.

The fabricated prototype was evaluated under CW excitation. For six frequency points within the operating band, the input power was swept from 20 dBm up to saturation. The measured DE and power gain versus output power and the saturated Pout, power gain, and DE at saturation and 10 dB OBO across the operating bandwidth are plotted in FIGURE 14.

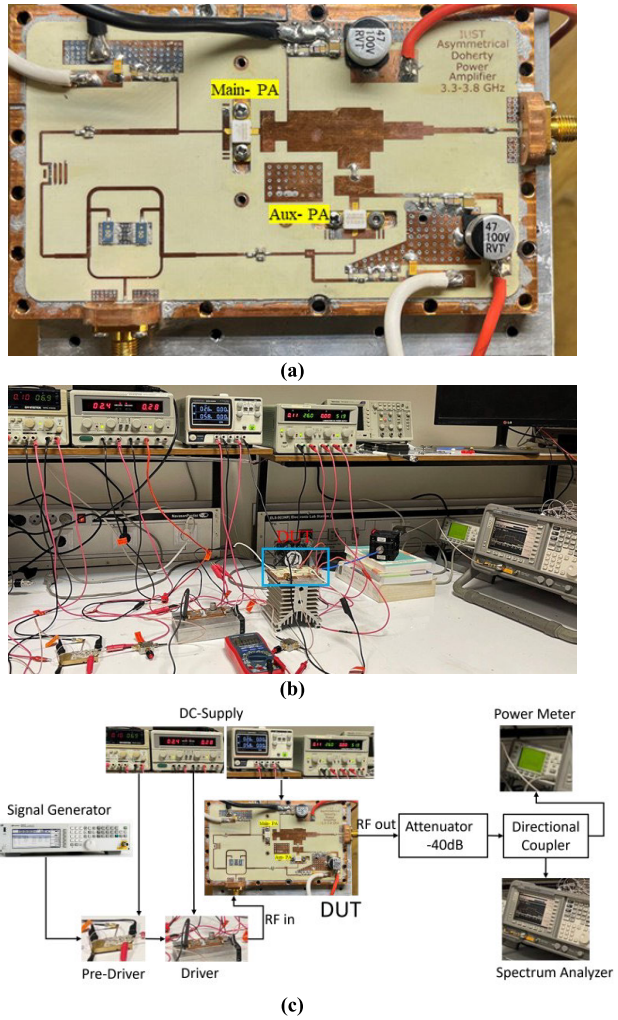

FIGURE 12. Photographs of (a) the fabricated Asymmetric DPA, (b) the measurement setup, and (c) the measurement setup description.

The saturated output power ranges from 46 dBm to 47.2 dBm, while the corresponding peak DE varies between 60.5% and 68.5%.

TABLE 3. Performance comparison with previously reported high-OBO PA in the 3-4 GHz band.

[Ref.] Year	Freq. (GHz)	Configuration (number of transistors)	FBW (%)	Single Carrier Test				Modulate Signal Test			
				OBO (dB)	DE in Doherty Region (%)	Pout @ Sat. (dBm)	DE @ Sat. (%)	Signal BW(MHz)	PAPR (dB)	P_{avg} (dBm)	ACPR (dBc)
[34] 2020	3.3-4.3	Symmetric DPA (2)	26.3	6	42.0-68.9[G]	43.2-44.5	58.6-68.9	LTE 20	7.2	37.2	-27
[13] 2022	3.45-3.75	Asymmetric DPA (2)	8.3	8.5	33.3- 62[G]	41.8-43.5	47-62[G]	5G-NR 100	8	36.8	-24.6
[25][P] 2022	3.1-4.2	LMBA (3)	30	10	37.5-65[G]	47.5-48.7	46-58[G]	5G-NR 100	10	37.8	-16
[10] 2023	3.3-4.2	Asymmetric DPA (2)	24.2	7.8	42.5-65[G]	42.4-42.8	57-65[G]	5G-NR 100	7.8	35	-27.2
[38] 2023	3.3-3.9	Symmetric DPA (2)	17	6	35-53.2[G]	45.6-47	48-53.2	NA	NA	NA	NA
[7] 2025	2.9-4.0	Asymmetric DPA (2)	32.3	8	43-71[G]	41.6-43.3	62.5-71.0[G]	5G-NR 100	7.9	35	-23.3
This work	3.3-3.8	Asymmetric DPA (2)	14.1	>9.5	45-69.6	46-47.3	60.5-68.5	5G-NR 20	12	35.2	-21
	3.4-3.8		11.1	>10							

[P] The results are presented under pulsed conditions with a duty cycle of 10%.
[G] Graphically estimated.
NA: Not available.

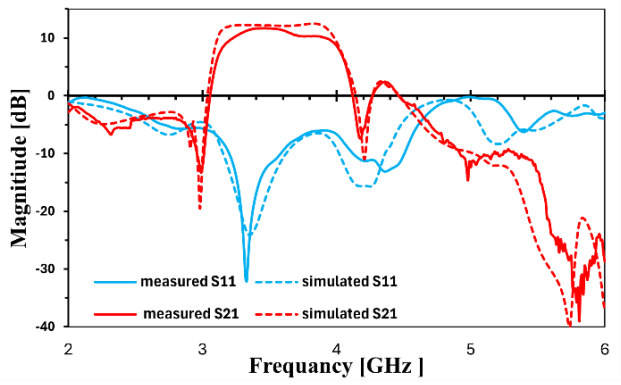

FIGURE 13. Comparison between measured and simulated S-parameters of the Asymmetric DPA.

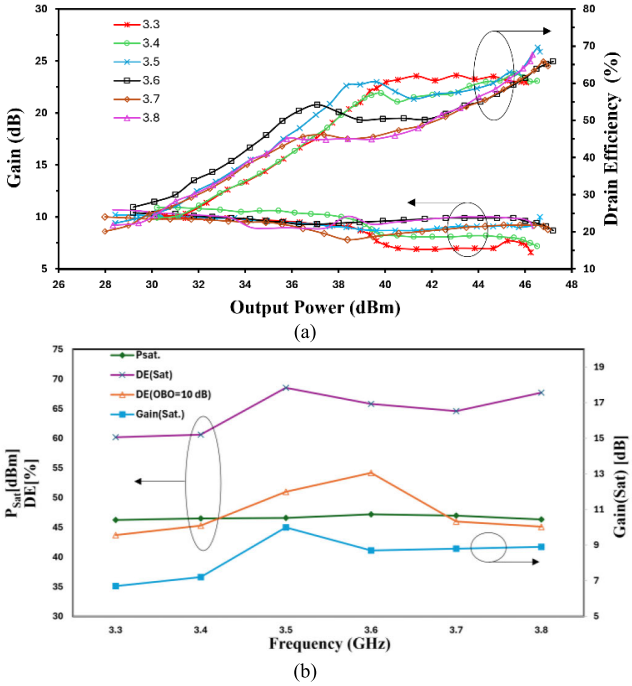

FIGURE 14. The measured performance of the fabricated DPA: (a) DE and gain versus output power, (b) saturated P_{out}, Gain, and DE at saturation and 10-dB OBO across the operating bandwidth.

Across the 3.3–3.8 GHz band, the DPA maintains a DE above 45 % for OBO levels exceeding 9.5 dB. A closer examination reveals that, except for the lower 100 MHz portion of the band, the DE remains above 45 % for OBO > 10 dB throughout 3.4–3.8 GHz.

The design target was a DE of approximately 50 % at 10-dB OBO. The fabricated prototype achieves a DE slightly below this target, primarily due to practical implementation factors such as non-ideal device behavior, passive-component losses, and fabrication tolerances. Nevertheless, the measured results confirm high efficiency and consistent performance over a wide bandwidth, validating both the proposed design methodology and the effectiveness of the TSM architecture.

To evaluate the performance of the asymmetric DPA under modulated-signal operation, a 5G-NR signal with a 20 MHz bandwidth and a 12 dB peak-to-average power ratio (PAPR) at a center frequency of 3.5 GHz was employed. Figure 15 shows the measured output power spectral density at an average output power of 35.2 dBm. the measured ACPR is approximately −21 dBc (−21.35 dBc and −20.83 dBc at the lower and upper adjacent channels, respectively) without applying digital predistortion (DPD), thereby reflecting the intrinsic linearity of the amplifier. Although this ACPR level represents the unlinearized performance of a highly efficient Doherty amplifier operating near saturation, practical 5G transmitter systems routinely employ digital predistortion (DPD), which can further improve linearity performance.

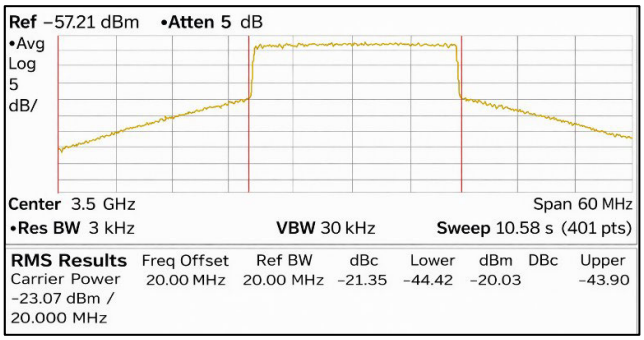

FIGURE 15. **The measured output power spectra density using a 20-MHz 5G-NR signal with 12-dB PAPR, at 3.5 GHz.**

The proposed amplifier is intended for sub-6 GHz 5G-NR base-station transmitters, where maintaining high efficiency over a large output back-off range is critical due to the high PAPR of OFDM signals. Under modulated-signal excitation, the amplifier achieves a measured average drain efficiency of 39.7%, demonstrating a favorable tradeoff between efficiency and linearity. Overall, these results confirm the suitability of the proposed DPA for energy-efficient wireless transmitter applications, while additional linearity improvement is expected when DPD is employed.

To position this work with respect to the state-of-the-art, the measured performance of the proposed amplifier is compared with several reported high-OBO power amplifiers operating within the 3–4 GHz band in TABLE 3. The primary objective of this design is to achieve high efficiency across a large Doherty region (approximately 10 dB OBO). The proposed amplifier maintains a drain efficiency higher than 45% within 9.5–10 dB OBO across the operating band. Among the previously reported works listed in TABLE 3, Ref. [25] demonstrates a comparable back-off range of 10 dB. However, as reported in [25], the efficiency decreases to approximately 37% in the middle of the OBO region. In contrast, owing to the proposed three-state matching technique, such mid-OBO efficiency degradation is significantly mitigated in the present work. Furthermore, Ref. [25] is based on a load-modulated balanced amplifier (LMBA) topology employing three active devices, whereas the proposed design utilizes a conventional two-device asymmetric Doherty architecture. This reduces circuit complexity and simplifies implementation and biasing while maintaining high back-off efficiency.

V. CONCLUSION

This paper presents a systematic design methodology for an asymmetric Doherty power amplifier (DPA) aimed at reducing the degradation of drain efficiency in the Doherty region. The method is based on the design of an output matching network (OMN) for the main amplifier, and its performance is investigated across three power regions: low power (LP), mid power (MP), and peak power (PP). To experimentally validate the proposed approach, an asymmetric Doherty amplifier operating in the 3.3 - 3.8 GHz frequency band has been designed and implemented. Measurement results demonstrate that the designed amplifier achieves a peak output power of 46-47.3 dBm and a drain efficiency (DE) exceeding 45% over a 10-dB OBO range, demonstrating a significant improvement compared to the prior works. Future research may explore the integration of intelligent adaptive control techniques, including neuromorphic and memristive circuits, for real-time nonlinearity compensation, dynamic impedance matching, and efficiency optimization in broadband Doherty power amplifiers operating under varying signal and load conditions [45], [46].

REFERENCES

[1] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. IRE*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.

[2] M. Iwamoto, A. Williams, P.-F. Chen, A. G. Metzger, L. E. Larson, and P. M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2472–2479, Dec. 2001.

[3] P. Colantonio, F. Giannini, R. Giofrè, and L. Piazzon, "The AB-C Doherty power amplifier. Part I: Theory," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 19, no. 3, pp. 293–306, May 2009.

[4] D. Y.-T. Wu and S. Boumaiza, "A mixed-technology asymmetrically biased extended and reconfigurable Doherty amplifier with improved power utilization factor," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1946–1956, May 2013.

[5] J. Xia, M. Yang, and A. Zhu, "Improved Doherty amplifier design with minimum phase delay in output matching network for wideband application," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 11, pp. 915–917, Nov. 2016.

[6] H. Oh, H. Kang, H. Lee, H. Koo, M. Kim, W. Lee, W. Lim, C.-S. Park, K. C. Hwang, K.-Y. Lee, and Y. Yang, "Doherty power amplifier based on the fundamental current ratio for asymmetric cells," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4190–4197, Nov. 2017.

[7] Y. Chen, W. Choi, J. Shin, H. Jeon, S. Bae, S. Bin, Y. Chan Choi, H. Oh, H. Kang, K.-Y. Lee, K. Cheol Hwang, and Y. Yang, "Simplified all-in-one load network of the broadband Doherty power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 73, no. 2, pp. 953–964, Feb. 2025.

[8] X. H. Fang and K.-K.-M. Cheng, "Extension of high-efficiency range of Doherty amplifier by using complex combining load," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2038–2047, Sep. 2014.

[9] J. Zhou, W. Chen, L. Chen, and Z. Feng, "3.5-GHz high-efficiency broadband asymmetric Doherty power amplifier for 5G applications," in *Proc. Int. Conf. Microw. Millim. Wave Technnol. (ICMMT)*, Sep. 2018, pp. 1–3.

[10] J. Shin, W. Choi, Y. Chen, H. Jeon, S. Bae, Y. C. Choi, H. Kang, H. Koo, Y. Y. Woo, K.-Y. Lee, K. C. Hwang, and Y. Yang, "Broadband virtual-stub Doherty power amplifier using asymmetric structure," *IEEE Access*, vol. 11, pp. 101425–101434, 2023.

[11] Y. Xu, J. Pang, X. Wang, and A. Zhu, "Enhancing bandwidth and back-off range of Doherty power amplifier with modified load modulation network," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 4, pp. 2291–2303, Apr. 2021.

[12] X. Ge, J. Qi, Z. Xie, T. Zhang, W. Kong, and J. Xia, "Design of asymmetric Doherty power amplifier based on 3-port output combinational network," in *Proc. IEEE Int. Workshop Electromagn., Appl. Student Innov. Competition (iWEM)*, Nov. 2021, pp. 1–3.

[13] Y. C. Choi, W. Choi, H. Oh, Y. Chen, J. Shin, H. Jeon, K. C. Hwang, K.-Y. Lee, and Y. Yang, "Doherty power amplifier with extended high-efficiency range based on the utilization of multiple output power back-off parameters," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 4, pp. 2258–2270, Apr. 2022.

[14] W. Choi, H. Kang, H. Oh, K. C. Hwang, K.-Y. Lee, and Y. Yang, "Doherty power amplifier based on asymmetric cells with complex combining load," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 4, pp. 2336–2344, Apr. 2021.

[15] A. Barthwal, K. Rawat, and S. Koul, "Bandwidth enhancement of three-stage Doherty power amplifier using symmetric devices," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 8, pp. 2399–2410, Aug. 2015.

[16] S. Chen, W. Wang, K. Xu, and G. Wang, "A reactance compensated three-device Doherty power amplifier for bandwidth and back-off range extension," *Wireless Commun. Mobile Comput.*, vol. 2018, no. 1, Jan. 2018, Art. no. 8418165.

[17] J. Xia, W. Chen, F. Meng, C. Yu, and X. Zhu, "Improved three-stage Doherty amplifier design with impedance compensation in load combiner for broadband applications," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 2, pp. 778–786, Feb. 2019.

[18] H. Golestaneh, F. A. Malekzadeh, and S. Boumaiza, "An extended-bandwidth three-way Doherty power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3318–3328, Sep. 2013.

[19] A. Barthwal, K. Rawat, and S. K. Koul, "A design strategy for bandwidth enhancement in three-stage Doherty power amplifier with extended dynamic range," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1024–1033, Feb. 2018.

[20] G. Liu, Z. Cheng, M. Zhang, S. Chen, and S. Gao, "Bandwidth enhancement of three-device Doherty power amplifier based on symmetric devices," *IEICE Electron. Exp.*, vol. 15, no. 3, 2018, Art. no. 20171222.

[21] Y. Cao and K. Chen, "Pseudo-Doherty load-modulated balanced amplifier with wide bandwidth and extended power back-off range," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 3172–3183, Jul. 2020.

[22] Z. Zhang, V. Fusco, Z. Cheng, C. Gu, N. Buchanan, and J. Ying, "A broadband Doherty-like power amplifier with large power back-off range," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 6, pp. 2722–2726, Jun. 2022.

[23] Y. Cao, H. Lyu, and K. Chen, "Wideband Doherty power amplifier in quasi-balanced configuration," in *Proc. IEEE 20th Wireless Microw. Technol. Conf. (WAMICON)*, Cocoa Beach, FL, USA, Apr. 2019, pp. 1–4.

[24] P. H. Pednekar, W. Hallberg, C. Fager, and T. W. Barton, "Analysis and design of a Doherty-like RF-input load modulated balanced amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5322–5335, Dec. 2018.

[25] P. Saad and R. Hou, "Symmetrical load modulated balanced power amplifier with asymmetrical output coupling for load modulation continuum," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 4, pp. 2315–2327, Apr. 2022.

[26] M. Akbarpour, M. Helaoui, and F. M. Ghannouchi, "A transformer-less load-modulated (TLLM) architecture for efficient wideband power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 9, pp. 2863–2874, Sep. 2012.

[27] D. Xiong, C. Liu, L. Huang, and H. Wang, "A 3.3–3.7 GHz broadband Doherty power amplifier," in *Proc. 13th Int. Symp. Antennas, Propag. EM Theory (ISAPE)*, Dec. 2021, pp. 1–3.

[28] S. Kim, J. Moon, J. Lee, Y. Park, D. Minn, and B. Kim, "Accurate offset line design of Doherty amplifier with compensation of peaking amplifier phase variation," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 10, pp. 3224–3231, Oct. 2016.

[29] R. Darraji and F. M. Ghannouchi, "Digital Doherty amplifier with enhanced efficiency and extended range," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 11, pp. 2898–2909, Nov. 2011.

[30] J. Pang, S. He, C. Huang, Z. Dai, J. Peng, and F. You, "A post-matching Doherty power amplifier employing low-order impedance inverters for broadband applications," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4061–4071, Dec. 2015.

[31] J. Pang, S. He, Z. Dai, C. Huang, J. Peng, and F. You, "Design of a post-matching asymmetric Doherty power amplifier for broadband applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 1, pp. 52–54, Jan. 2016.

[32] X. Y. Zhou, S. Y. Zheng, W. S. Chan, S. Chen, and D. Ho, "Broadband efficiency-enhanced mutually coupled harmonic postmatching Doherty power amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 7, pp. 1758–1771, Jul. 2017.

[33] X. Y. Zhou, S. Y. Zheng, W. S. Chan, X. Fang, and D. Ho, "Post-matching Doherty power amplifier with extended back-off range based on self-generated harmonic injection," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 4, pp. 1951–1963, Apr. 2018.

[34] C. Shen, S. He, X. Zhu, J. Peng, and T. Cao, "A 3.3–4.3-GHz high-efficiency broadband Doherty power amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 11, pp. 1081–1084, Nov. 2020.

[35] S. Rafati, V. Nayyeri, and M. Soleimani, "A 100-W Doherty power amplifier with super-octave bandwidth," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 6, pp. 1009–1013, Jun. 2020.

[36] M. Ghazizadeh and V. Nayyeri, "Design of a 50-W power amplifier with two-octave bandwidth and high-efficiency using a systematic optimization approach," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 5, pp. 501–504, May 2021.

[37] M. Ghazizadeh, S.-H. Javid-Hosseini, and V. Nayyeri, "A 90W 1-3 GHz power amplifier module," in *Proc. 50th Eur. Microw. Conf. (EuMC)*, Jan. 2021, pp. 17–20.

[38] M. Shahmoradi, S.-H. Javid-Hosseini, V. Nayyeri, R. Giofré, and P. Colantonio, "A broadband Doherty power amplifier for sub-6 GHz 5G applications," *IEEE Access*, vol. 11, pp. 28771–28780, 2023.

[39] Y. Zhuang, Z. Fei, A. Chen, Y. Huang, K. Rabbi, and J. Zhou, "Design of multioctave high-efficiency power amplifiers using stochastic reduced order models," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1015–1023, Feb. 2018.

[40] P. Jia, F. You, S. He, and X. Qian, "A 0.25–1.25-GHz high-efficiency power amplifier with computer-aided design based on optimized impedance solution continuum," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 5, pp. 443–445, May 2018.

[41] S. Dudkiewicz, M. S. Tenberge, G. Esposito, and T. Barbieri, "Understanding the relevance of harmonic impedance matching in amplifier design," *IEEE Microw. Mag.*, vol. 58, no. 4, pp. 112–122, Apr. 2015.

[42] P. Colantonio, F. Giannini, R. Giofré, E. Limiti, A. Serino, M. Peroni, P. Romanini, and C. Proietti, "A C-band high-efficiency second-harmonic-tuned hybrid power amplifier in GaN technnology," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 6, pp. 2713–2722, Jun. 2006.

[43] X. Y. Zhou, W. S. Chan, D. Ho, and S. Y. Zheng, "Loading the third harmonic: A linear and efficient post-matching Doherty PA," *IEEE Microw. Mag.*, vol. 19, no. 1, pp. 99–105, Jan. 2018.

[44] U. H. Gysel, "A new N-way power divider/combiner suitable for high-power applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Feb. 1975, pp. 116–118.

[45] S. Gao, F. Shi, X. Xu, J. Chen, H. H.-C. Iu, Y. Cao, L. Qin, and J. Mou, "A memristor-based neural network circuit with classical conditioning and fear generalization," *IEEE Trans. Consum. Electron.*, vol. 72, no. 2, pp. 3213–3224, May 2026.

[46] S. Gao, Y. Song, Y. Cao, H. H.-C. Iu, L. Qin, Y. Zhang, and J. Mou, "Biologically plausible memristive decision-making circuit for adaptive control in industrial autonomous navigation," *IEEE Trans. Ind. Informat.*, vol. 22, no. 6, pp. 4801–4812, Jun. 2026.

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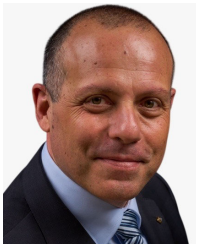

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