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High-Efficiency MMIC GaN RF Power Amplifier With Improved Linearity in Series–Parallel Configuration

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ABSTRACT This paper presents a series-parallel RF power amplifier (PA) configuration with improved linearity performance achieved through an optimal combination of gate bias voltages and input power levels. The fundamental output voltage and the total third-order intermodulation distortion (IMD3) expressions of the series-parallel PA are analytically derived. Moreover, the proposed algorithm systematically determines optimal gate bias combinations for driver and power stages through comprehensive device characterization, harmonic balance simulations, and vector-based IMD3 cancellation analysis to maximize the achievable performance in terms of both linearity and efficiency. In addition, the fundamental and harmonic transconductances for different transistor active areas have been analyzed. This analysis determines the suitable number of gate fingers N_f and gate width W_f of the transistor in both driver and final stages to fulfill the required output power level, considering linearity and efficiency performance requirements. A 2-W X-band high linear and efficient RF PA is designed and fabricated in a $0.15-\mu$m GaN-on-SiC process. A good agreement between simulations and measurements has been achieved. The continuous wave measurements of the proposed PA showed a power gain of 19 dB, a saturated output power level of more than 34-dBm, together with a power added efficiency (PAE) of 40% at 1-dB compression point. The two-tone signal measurements showed a similar gain level with a PAE of more than 37% at 33.5-dBm of output power. Moreover, the IMD3 is below −30-dBc while the PAE is greater than 33%. Modulated measurements using a 5-MHz WCDMA signal (PAPR = 3.5 dB) confirmed the PA linearity improvement perfomance, showing an adjacent channel power ratio (ACPR) of -27 dBc and an error vector magnitude (EVM) between 1.9 and 5.1% across its output power range, making it suitable for high-order modulation schemes. The results validate the proposed design approach, offering competitive performance with respect to the actual state of the art 6G communication systems by balancing efficiency, linearity, and reliability.

INDEX TERMS Communication systems, GaN, high efficiency, linearity, MMIC, power amplifiers, RFPA, X-band, 6G.

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I. INTRODUCTION

Telecommunication systems ask for RF power amplifiers (PAs) capable of operating with high efficiency and linearity

while providing the required output power level to accommodate the increasing demand of high-speed data transmission, extended network coverage, and seamless connectivity [1], [2], [3], [4].

In recent years, the World Radio Communication Conferences (WRC) and the International Telecommunication Union (ITU) have added spectrum bands to meet the needs of increasing transmission rates; 6 G systems will be able to transmit and receive signals within multiple different frequency range set in the identified lower- (380 MHz-1 GHz), mid- (1 GHz—24 GHz), and higher-band (24 GHz - *to* GHz). There has been interest in the market in pursuing future spectrum for 6 G within mid and higher bands. This opens the door for market and researchers interested in pursuing future spectrum options for the 6 G wireless systems [2], [5], [6]. Gallium Nitride (GaN) technology has attractive properties including high electron mobility, wide band gap, and high power handling capabilities, positioning it as a transformative force in the evolution of 6 G wireless communications. The transition to 6 G introduces a lot of complexities and performance requirements that endure massive pressure on RF PA designers. These requirements include higher operating frequency, wider bandwidths, and enhanced linearity, coupled with stringent power efficiency and compact form factor demands. This presents a formidable challenge for traditional RF PA architectures [7], [8], [9], [10], [11], [12], [13].

The significance of RF PAs linearity cannot be understated, particularly in the context of advanced wireless applications. Linearity dictates the ability of the PA to reproduce an amplifier version of the input signal without introducing distortions or nonlinearities, thereby ensuring the fidelity and accuracy of the transmitted information. In pursuing higher data rates, increased spectral efficiency, and seamless connectivity, the stringent demands placed on PA to maintain exceptional linearity performance become increasingly paramount. At system level, to overcome device nonlinearities, several linearization strategies such as harmonic injection, feed-forward, analog post-distortion, active predistorter, digital pre-distortion, and cartesian loop feedback, are typically adopted [14], [15], [16], [17], [18]. However, the main drawback of these techniques is the need for extra auxiliary circuits, which may increase circuit complexity and power consumption.

In [19], the single transistor is partitioned into sub-cells, and each cell is biased separately. The phase of the third-order intermodulation (IMD3) is changed with the gate bias voltage, which is used to generate the anti-phase of IM3 at the combined output node of the device to improve the linearity performance. Authors in [20] utilize a MOS driver stage, which is biased in the sub-threshold region with anti-phase of the CMOS PA of the power stage as a cascaded structure. The disadvantage of this method is that the driver is biased in class C, which means that the transistor is off and uses a portion of the RF input power to start conducting. In addition, the series configuration is less reliable

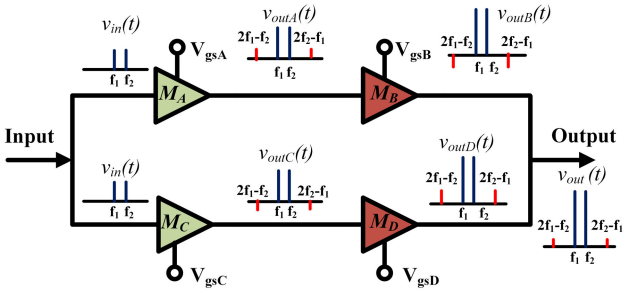


FIGURE 1. Simplified schematic of the proposed series-parallel power amplifier configuration.

because failure at any stage results in total output power loss.

The anti-phase IM3 linearity improvement techniques, widely used in CMOS and HBT technologies, are developed depending on the class of operation (gate bias) of the driver and power stages, such that an opposite-signed IMD3 between the drive and power stages is obtained [20], [21]. In [22] and [23], the parallel transistor configuration for improving the linearity at the maximum achievable efficiency level or achieving high linearity levels with improved efficiency is discussed. However, the main drawback of this technique is that the linearity improvement depends on the two branches working simultaneously. All the techniques mentioned above discuss linearity improvement, depending on the variation of gate bias only, without providing a clear algorithm suitable for selecting the gate bias points that improve the linearity. Moreover, such approaches discuss only either series or parallel PA configuration without taking into consideration the effects of both gate bias and input power changes to improve linearity without sacrificing efficiency.

In this paper, the linearity of the series-parallel configuration is studied and analyzed to obtain a more reliable, highly linear, and efficient PA design. The proposed architecture, reported in Fig. 1, is composed of two parallel combined branches, with each branch consisting of a series driver and a power stage. The main target of this work is to improve the linearity of each branch by selecting the correct combination of the previously studied optimum efficiency bias points, and then the linearity of the overall parallel PA will be improved similarly. Therefore, once good linearity and efficiency performance have been achieved in each series arm, in case of failure occurrence at any parallel branch, the output power is only degraded while maintaining a good linearity and efficiency behavior. The variation of the IM3 phase based on two parameters, gate bias voltage and input power level, is discussed. Thereby, transistor profile data sets visualization for the driver and power stages is created by sweeping gate bias and input power level. Afterwards, an algorithm is developed to select the best combination of the driver and power stage gate voltages to improve linearity at the optimum efficiency and power level for the complete series-parallel PA. The design approach has been verified by the implementation and fabrication of a 2-W MMIC PA in the X-Band.

The paper is structured as follows: Section II discusses the proposed theoretical analysis and the design approach, while the design implementation of the 2-W PA to experimentally verify the proposed method is discussed in Section III. Section IV reports the measurement results of the realized prototype and compares them with the state-of-the-art ones. Finally, conclusions are drawn in Section V.

II. THEORETICAL ANALYSIS AND DESIGN METHODOLOGY OF THE PROPOSED ARCHITECTURE

This section evaluates the linearity performance of the combined driver and power stages by investigating two key parameters: gate bias voltage and input power level. Adopting the approach outlined in [23], we derive analytical expressions for the fundamental and third-order intermodulation (IM3) voltages in the proposed series-parallel PA design. Furthermore, the detailed transistor profile datasets are compiled for both the driver and power stages. Additionally, an optimization algorithm is introduced to identify the optimal gate bias voltage combination for the two-stage series-parallel configuration.

A. THEORETICAL ANALYSIS

The proposed series-parallel PA configuration is illustrated in Fig. 1. This architecture focuses on the linearity enhancement at two levels: first, for each branch consisting of a driver (M_A/M_C) and power stage (M_B/M_D) pair, and second, for the overall PA after combining both branches. Analysis begins with deriving the fundamental and IM3 voltage components of the M_A driver and M_B power stage in a cascaded configuration. Using Volterra series expansion, the characterization of the nonlinear transfer function of the complete PA system (upper and lower branches with driver and PA stage for each) is expressed as:

$$v_{in}(t) = A(cosw_1 t + cosw_2 t) \tag{1}$$

$$v_{out_A}(t) = a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 \tag{2}$$

$$v_{out_C}(t) = c_1 v_{in} + c_2 v_{in}^2 + c_3 v_{in}^3 \tag{3}$$

$$v_{out_B}(t) = b_1 v_{out_A} + b_2 v_{out_A}^2 + b_3 v_{out_A}^3 \tag{4}$$

$$v_{out_D}(t) = d_1 v_{out_C} + d_2 v_{out_C}^2 + d_3 v_{out_C}^3 \tag{5}$$

where a_i, b_i, c_i, d_i represent the power series coefficients for transistors M_A, M_B, M_C and M_D respectively, with $i = 1, 2, \ldots$ denotes the nonlinearity order. Similarly, $v_{in}(t)$ is the overall input voltage, while $v_{out_A}(t)$, $v_{out_B}(t)$, $v_{out_C}(t)$ and $v_{out_D}(t)$ are the output voltages of driver M_A, power stage M_B, driver M_C and power stage M_D, respectively. Referring to Fig. 1, the total fundamental voltage component of the power amplifier is obtained by combining both arms ($v_{out_B}(t)$ and $v_{out_D}(t)$) as:

$$\begin{aligned} v_{\text{out}}(\omega_{1,2}t) = &\left[\left(a_1 b_1 + \frac{9}{4}a_3 b_1 A^2 + \frac{9}{4}a_1^3 b_3 A^2\right)A \right. \\ &\left. + \left(c_1 d_1 + \frac{9}{4}c_3 d_1 A^2 + \frac{9}{4}c_1^3 d_3 A^2\right)A\right] \\ &\times (\cos\omega_1 t + \cos\omega_2 t) \end{aligned} \tag{6}$$

In (6), the overall gain expansion/compression depends on the fundamental and third-order coefficients of the power series of both driver and power stages. Therefore, the linearity performance of the overall PA can be enhanced by carefully selecting such terms of the power series. Thereby, the total IM3 voltage of the proposed configuration can be expressed as:

$$\begin{aligned} v_{\text{out}}(2\omega_1 - \omega_2)t = &\left[\left(\frac{3}{4}a_3 b_1 + \frac{3}{4}a_3^3 b_3\right)A^3 \right. \\ &\left. + \left(\frac{3}{4}c_3 d_1 + \frac{3}{4}c_3^3 d_3\right)A^3\right] \\ &\times \cos(2\omega_1 - \omega_2)t \end{aligned} \tag{7}$$

As demonstrated in (7), the total IM3 distortion is determined by the third-order terms of the power series expansion. These terms exhibit the same dependence on gate bias and input power level as the third-order current coefficients. Therefore, the total IM3 can be minimized when the third-order coefficients of the driver and power stages in (7) are properly phased out to achieve cancellation.

Based on these findings, an optimization algorithm that determines the gate bias voltage combination that simultaneously maximizes linearity and power efficiency for both individual branches and the complete PA system is proposed in Subsection II-B. The algorithm's implementation and performance are discussed in detail.

B. DESIGN METHODOLOGY

Fig. 2 presents the workflow of the proposed design methodology for linearity/efficiency enhancement of RF power amplifiers.

Steps 1 and 2: The design algorithm starts with geometric optimization of the active devices, determining the optimal gate width (W_f) and number of fingers (N_f) for both driver and power stages to achieve the specified output power (P_{out}). The characterization begins with DC analysis, where gate bias voltage sweeps ($V_{GS} \in [V_{\min}, V_{\max}]$) establish the operating class (typically Class-AB or B) and quiescent point $Q(V_{GSQ}, I_{DQ})$. Subsequent small-signal analysis evaluates the transconductance components (G_{m1} for fundamental response and G_{m2}, G_{m3} for harmonics) across the design space of devices' geometry ($W_f \times N_f$ combinations). The DC and small-signal analysis alone are inadequate for comprehensive linearity assessment, as transconductance terms are strongly affected by input power levels. To address this, a multi-parametric dataset is generated for each device configuration through Harmonic Balance (HB) simulations, incorporating load/source-pull techniques up to 3 dB gain compression.This dataset quantitatively relates efficiency and linearity metrics to gate bias and input power, enabling co-optimization of power performance and distortion characteristics.

In addition, one- and two-tone simulations by sweeping input power and gate bias are performed by terminating each device (driver and power stages) with the input and output

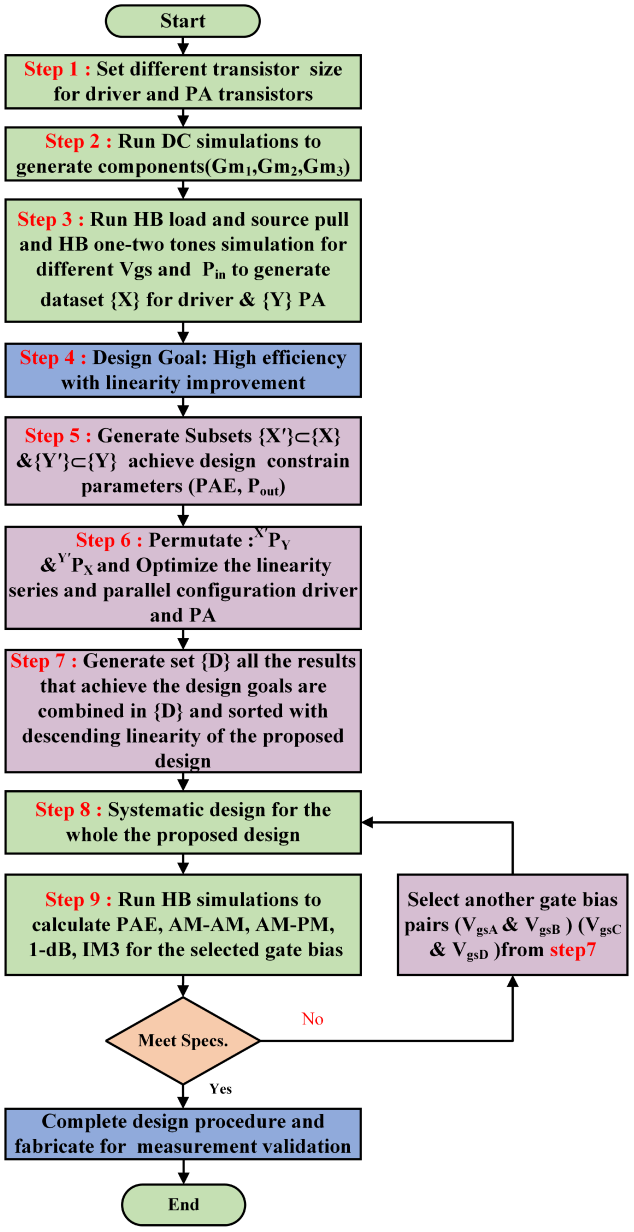


FIGURE 2. The flow chart of the proposed methodology.

optimum impedances generated from load and source pull analysis.

Step 3: Comprehensive efficiency and linearity characterization datasets are generated for both the driver stage, named as $\{X\}$, and the power stage, named as $\{Y\}$, quantifying:

- Power gain (G_p)
- Power-added efficiency (PAE)
- Output power (P_{out})
- AM-AM distortion characteristics
- Third-order intermodulation products (IM3)

The resulting datasets provide a systematic evaluation of each stage's behavior across varying input power levels and gate bias, facilitating detailed performance analysis and optimization.

Step 4: The proposed algorithm is applied to determine the best gate bias voltage combination for the proposed configuration to achieve the design goals. The proposed algorithm is created to provide a highly efficient RF PA with the best achievable linearity based on the phase cancellation technique and the linearization strategy employed:

1) Power stage optimization: Gate biases are tuned to achieve a 180° phase difference in IM3 components between parallel power cells.
2) Driver stage synchronization: Each driver's operating point is optimized to complement its corresponding power stage's nonlinearity profile.
3) Superposition: The combined output exhibits destructive interference of IM3 components:

$$IM3_{\text{total}} = \left\| IM3_1 e^{j\phi_1} + IM3_2 e^{j\phi_2} \right\| \ll IM3_{\text{individual}} \quad (8)$$

Step 5: Constrained design spaces $\{\bar{X}\}$ and $\{\bar{Y}\}$ are generated while the power amplifier parameters are stratified by designer constraints by applying:

$$\bar{X} = \{\bar{X} \in X \,|\, \text{PAE}, P_{out}, G_P \geq \text{spec}\} \quad (9)$$

$$\bar{Y} = \{\bar{Y} \in Y \,|\, \text{PAE}, P_{out}, G_P \geq \text{spec}\} \quad (10)$$

Step 6: Linearity optimization; the linearity of the proposed configuration is enhanced through a cross-permutation process between the driver and power stages. This cross-parameter exploration identifies optimal combinations that minimize nonlinear distortion. The linearity optimization employs a permutation operator P_{erm} acting on the parameter spaces:

$$P_{\text{erm}} : \bar{X} \times Y \cup \bar{Y} \times X \rightarrow \mathbb{R}^n \quad (11)$$

where:

- $\bar{X} \subset X$ are the constrained driver stage parameters
- $\bar{Y} \subset Y$ are the constrained power stage parameters
- The operation generates an n-dimensional matrix.

The linearity performance of the proposed design can be improved in two steps. The first step is selecting the gate bias of the power stage in each arm to obtain the IM3 out of phase for two parallel power stages. The second step is determining the driver's gate bias to be out of phase with its power stage to obtain high linear performance in each branch individually. Then, the two arms are combined, and the total IM3 is calculated to obtain the lowest value, thus achieving a highly linear performance of the proposed PA.

The best gate biases of M_B and M_D (power stage gate biases) are computed after calculating the variance of the power stage $IM3_{PAstage}$ by permuting $\{X\}$ by $\{\bar{X}\}$ as follows,

$$\sigma_{\text{IM3,PA stage}} = \left\| IM3_X e^{j\phi_X} + IM3_{\bar{X}} e^{j\phi_{\bar{X}}} \right\| \quad (12)$$

where $IM3_X$ is the IM3 for the power stage dataset and $IM3_{\bar{X}}$ is the highest efficiency gate bias in $\{X\}$.

The resultant data set $\{Z\}$ is generated and sorted for the optimal pair gate bias combination (M_B and M_D), including linearity/efficiency parameters such as PAE, Gain, and $\sigma_{IM3,PAstage}$ for the parallel configuration.

Concerning the driver stages, the gate bias of each branch (M_A and M_C) is determined based on (13) and (14) to obtain lower linearity values for the series path $IM3_{AB}$ for (M_A and M_B) and $IM3_{CD}$ for (M_C and M_D). The total IM3 for each branch is:

$$IM3_{AB} = \left\| IM3_Y e^{j\phi_Y} + IM3_{\bar{X}_B} e^{j\phi_{\bar{X}_B}} \right\| \tag{13}$$

$$IM3_{CD} = \left\| IM3_Y e^{j\phi_Y} + IM3_{\bar{X}_D} e^{j\phi_{\bar{X}_D}} \right\| \tag{14}$$

where $IM3_{AB}$ is the total IM3 of the upper series branch (driver M_A and power stage M_B) and $IM3_{CD}$ is the total IM3 of the lower series branch (driver M_C and power stage M_D) with respective phase $\phi_{\bar{X}_B}$ and $\phi_{\bar{X}_D}$, while $IM3_Y$ is the IM3 of $\{Y\}$ for different gate bias of PA stage with phase ϕ_Y and $IM3_{\bar{X}_B}$ and $IM3_{\bar{X}_D}$ are the IM3 of the selected gate bias of power stages for parallel configuration from the optimized dataset $\{Z\}$. The final linearity is evaluated by combining the IM3 of both branches by vector summation.

Step 7: The final dataset $\{D\}$ is generated and sorted, containing the optimal gate bias combinations for all transistors (M_A, M_B, M_C and M_D) and the linearity/efficiency parameters such as $\sigma_{IM3,PA}$, PAE_{total}, G_{total}, and $P_{out,total}$ for the proposed configuration. They are:

$$\sigma_{IM3,PA} = IM3_{AB} + IM3_{CD} \tag{15}$$

$$PAE_{AB} = \frac{G_B PAE_A PAE_B}{G_B PAE_A + PAE_B} \tag{16}$$

$$PAE_{CD} = \frac{G_D PAE_C PAE_D}{G_D PAE_C + PAE_D} \tag{17}$$

$$PAE_{total} = \frac{1}{2}\left(\frac{G_B PAE_A PAE_B}{G_B PAE_A + PAE_B} + \frac{G_D PAE_C PAE_D}{G_D PAE_C + PAE_D} \right) \tag{18}$$

$$G_{total} = \frac{1}{2}\sum_{i=A}^{D} G_i \tag{19}$$

$$P_{out,total} = \eta_{\text{comb}}(P_{out,B} + P_{out,D}) \tag{20}$$

where $PAE_{A,B,C,D}$, $G_{A,B,C,D}$ are the PAE and gain of each stage, respectively. In addition, $P_{out,B,D}$ is the output power of each branch, and η_{comb} is the combiner efficiency, which takes into consideration the losses of the combiner. These equations do not account for passive losses in the matching circuits. Designers should include an estimated loss margin when setting the output power target, based on the expected losses in the matching network. As a result, the best pair gate bias of the proposed configuration that achieves the design goal of high linearity with the best achievable efficiency under certain constraints is obtained and sorted in the dataset $\{D\}$.

The proposed algorithm employs a systematic brute-force search to evaluate all feasible gate bias combinations for the driver and power stages, ensuring optimal linearity and efficiency trade-offs. As detailed in Algorithm 1, the process begins by generating constrained subsets $\bar{X}$ and $\bar{Y}$ from the transistor characterization datasets, filtering for gate bias conditions that meet minimum PAE (> 40%), gain (> 10 dB), and output power specifications.

A performance matrix $\{Z\}$ is constructed through exhaustive permutation of power stage biases (V_{gs_B}, V_{gs_D}) to identify pairs that minimize parallel IM3 distortion via vector cancellation (Eq. 12). The algorithm then iterates over driver-stage biases (V_{gs_A}, V_{gs_C}) in combination with the top-performing power-stage pairs from $\{Z\}$, computing:

- The total IM3 distortion for each series branch ($IM3_{AB}$, $IM3_{CD}$) using Eqs. 13–14,

Algorithm 1 Series-Parallel PA Bias Optimization With Performance Matrix Generation

Require:
Driver dataset $\{X\}$: $(V_{gs}, P_{in}, G, PAE, IM3, \phi_{IM3})$
Power dataset $\{Y\}$: $(V_{gs}, P_{in}, G, PAE, IM3, \phi_{IM3})$

Ensure:
Performance matrix $\{D\}$: $(V_{gsA}, V_{gsB}, V_{gsC}, V_{gsD}, P_{in}, PAE_{total}, G_{total}, P_{out}, \sigma_{IM3})$

// Step 1: Generate constrained subsets (Eq. 9-10)
$\bar{X} \leftarrow \{(V_{gs}, P_{in}) \in X \mid PAE \geq 40\%, G \geq 10\text{dB}, P_{out} \geq 24\text{dBm}\}$
$\bar{Y} \leftarrow \{(V_{gs}, P_{in}) \in Y \mid PAE \geq 40\%, G \geq 10\text{dB}, P_{out} \geq 31\text{dBm}\}$
// Step 2: Parallel branch optimization (Eq. 12)
Initialize $\{Z\} \leftarrow \emptyset$
for $(V_{gsB}, P_{inB}), (V_{gsD}, P_{inD}) \in \bar{X} \times X$ **do**
  $\sigma_{IM3}^{par} \leftarrow \|IM3_B e^{j\phi_B} + IM3_D e^{j\phi_D}\|$
  $PAE_{par} \leftarrow \frac{1}{2}(PAE_B + PAE_D)$
  Add $(V_{gsB}, V_{gsD}, P_{inB}, \sigma_{IM3}^{par}, PAE_{par})$ to $\{Z\}$
Sort $\{Z\}$ by σ_{IM3}^{par} (ascending) and PAE_{par} (descending)
// Step 3: Series branch optimization (Eq. 13-14)
Initialize $\{D\} \leftarrow \emptyset$
for $(V_{gsA}, P_{inA}), (V_{gsC}, P_{inC}) \in \bar{X} \times Y$ **do**
  for top (V_{gsB}, V_{gsD}) pairs from $\{Z\}$ **do**
    $IM3_{AB} \leftarrow \|IM3_A e^{j\phi_A} + IM3_B e^{j\phi_B}\|$
    $IM3_{CD} \leftarrow \|IM3_C e^{j\phi_C} + IM3_D e^{j\phi_D}\|$
    $\sigma_{IM3}^{total} \leftarrow IM3_{AB} + IM3_{CD}$ % *Eq. 15*
    $PAE_{total} \leftarrow \frac{1}{2}\left(\frac{G_B PAE_A PAE_B}{G_B PAE_A + PAE_B} + \frac{G_D PAE_C PAE_D}{G_D PAE_C + PAE_D}\right)$
    $G_{total} \leftarrow \frac{1}{2}(G_A + G_B + G_C + G_D)$
    $P_{out,total} \leftarrow \eta_{comb}(P_{out,B} + P_{out,D})$
    Add $(V_{gsA}, V_{gsB}, V_{gsC}, V_{gsD}, P_{in}, PAE_{total}, G_{total}, P_{out}, \sigma_{IM3}^{total})$ to $\{D\}$
// Step 4: Final selection
Sort $\{D\}$ by:
  1. σ_{IM3}^{total} (ascending) % *Prioritize linearity*
  2. PAE_{total} (descending) % *Then efficiency*
Select top configuration from $\{D\}$
return $\{D\}$ with columns: $[V_{gsA}, V_{gsB}, V_{gsC}, V_{gsD} | P_{in} | PAE_{total} | G_{total} | P_{out} | \sigma_{IM3}^{total}]$
// Step 5: Verification (Section III-B)
Simulate PAE, AM-AM/PM, IMD3 for selected biases
Compare with measurement results (Figs. 13-23)

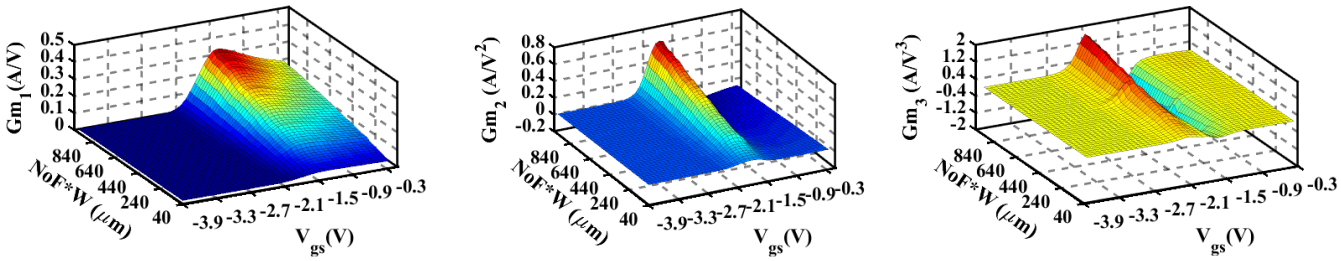


FIGURE 3. The DC simulation result of the transconductance (a) Gm_1, (b) Gm_2, (c) Gm_3.

- The overall PA efficiency (PAE_{total}) and gain (G_{total}) via Eqs. 16–19,
- The total output power ($P_{out,total}$) accounting for combiner losses (Eq. 20).

These results populate the final design matrix $\{D\}$, enabling optimal bias selection for linearity-efficiency trade-offs. This computationally intensive approach guarantees globally optimal bias selection by explicitly evaluating the design space, as opposed to heuristic methods that may converge to local optima.

Steps 8 and 9: The systematic design for the whole proposed configuration to verify the proposed methodology. Moreover, the pair's gate bias can be changed from the $\{D\}$ if there is a deviation from the predicted design due to the degree of freedom of the proposed methodology.

The accuracy of the simulations, and consequently the integrity of the overall design, is contingent upon the fidelity of the active device model. In this work, the large-signal behavior is represented using the Win Semiconductors 0.15-μm GaN HEMT foundry PDK model. This production-grade, physics-based model captures the dominant nonlinear mechanisms—most notably self-heating and charge-trapping—through a set of comprehensive and well-validated subcircuit formulations.

The next section presents the design and implementation of a 2−W GaN MMIC power amplifier based on the approach discussed.

III. DESIGN & VERIFICATION OF A 2-WATT GaN MMIC PA

This section presents the design, verification, and implementation of the proposed design methodology for a 2−W GaN MMIC PA operating from 10.4 to 10.8 GHz in 6G communication systems. The design utilizes a 0.15-μm GaN HEMT process (Win Semiconductor) that delivers optimal performance for X-band power applications and focuses on optimizing both efficiency and linearity through systematic gate bias configuration. The validity of the simulations and the subsequent design relies on the active device model. The large-signal model used is the Win Semiconductors 0.15-μm GaN HEMT Foundry PDK Model. This production-grade, physics-based model incorporates key nonlinear phenomena, including self-heating and charge trapping effects, through comprehensive sub-circuits. This technology combines high electron mobility ($>2000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) with excellent thermal conductivity ($490\,\mathrm{W\,m^{-1}\,K^{-1}}$) and breakdown characteristics 120 V, enabling simultaneous high-efficiency and linearity operation. The process's low on-resistance (2.2 Ωmm) and high current density ($985\,\mathrm{mA\,mm^{-1}}$) further support the power stage requirements, while its 30 GHz f_T ensures robust gain at the targeted frequency band (10.4 GHz to 10.8 GHz).

A. TRANSISTOR SIZING, NONLINEARITY ANALYSIS, AND BIAS OPTIMIZATION

Based on the previous analysis, the transistor size (gate width and number of fingers) is determined for both driver and power stages to achieve the required output power level. The fundamental and higher-order transconductances are simulated for different device geometries, and the total gate periphery ($N_f * W_f$) is varied from 60 to 1000 μm. Fig. 3 reports the behaviors of fundamental, second and third order transconductances as functions of the gate periphery and gate bias voltage (V_{gs}) from $Vgs_{\min} = -3.9$ to $Vgs_{\max} = -0.3$V at a drain voltage of 28 V. Fig. 3 illustrates that the linear transconductance (Gm_1) increases as the total gate periphery increases, while the second- and third-order transconductance (Gm_2 and Gm_3) show that the nonlinearity increases as the total gate periphery increases. Moreover, Gm_2 and Gm_3 vary from positive to negative values depending on the gate bias voltage.

The total gate width of the transistors in the power and driver stages should be determined to achieve an output power greater than 1 W from each branch in Fig. 1, ensuring a total output power of 2 W. The output power target was set higher to compensate for the estimated passive losses in the matching networks and power combiner. To satisfy this goal, the power stage uses a 4×100 μm, while the driver stage uses 4×50 μm. The multi-finger design provides three key advantages: (1) minimized current crowding and self-heating through width distribution, (2) reduced gate resistance (R_g) for improved high-frequency response, and (3) optimal balance between parasitic capacitances (C_{gs}, C_{gd}) and thermal impedance. The $N_f = 4$ selection represents the optimal compromise between power handling

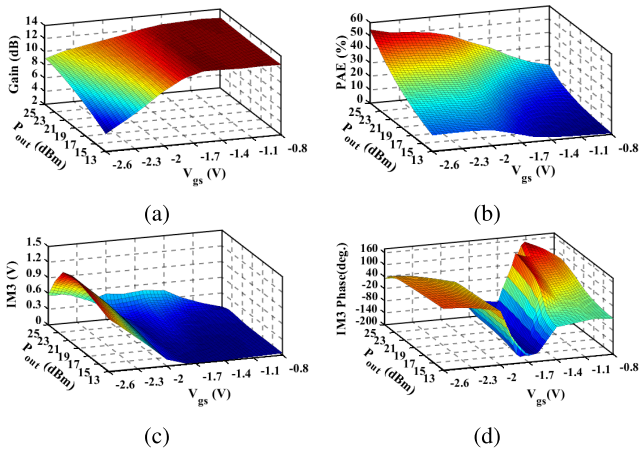


FIGURE 4. The transistor profile of the driver stage (a) Gain (b) PAE (c) IM3 level (d) IM3 phase.

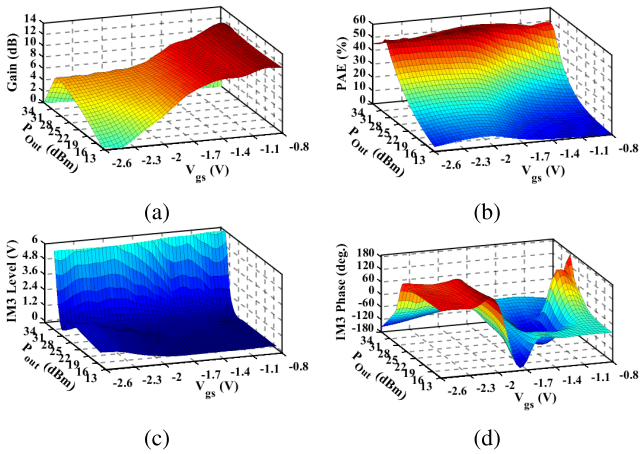


FIGURE 5. The transistor profile of the power stage (a) Gain (b) PAE (c) IM3 level (d) IM3 phase.

capability, thermal management, and impedance matching requirements.

The DC analysis is performed by sweeping the gate bias from −2.6V to −0.8V with a step $\Delta V_{gs} = 0.1$ V to determine the class of operation from class A to class C. The drain bias voltage is fixed to 28V for both driver and power stages. To populate the datasets of both driver and power transistors, HB source and load pull simulations at center frequency (10.6 GHz) and up to 3dB of gain compression have been carried out. Subsequently, the input and output impedance generated from such source/load-pull analysis are recorded at each gate bias voltage and input power level. Afterwards, one and two-tone simulations were conducted to obtain linearity/efficiency parameters such as power Gain, PAE, IM3 amplitude, and IM3 phase. Finally, the transistor datasets containing the linearity/efficiency characterization are generated for the driver stage $\{X\}$ and power stage $\{Y\}$. Fig. 4 and Fig. 5 show the power gain, PAE, and IM3 amplitude and IM3 phase at different output power and gate bias voltage for both driver and power stages. The simulation results are reported at 3dB of gain compression for each gate bias voltage while the two-tone spacing is set to 10MHz. As expected, class C biased devices achieve the lowest linearity (highest IM3) and the highest PAE value. The latter is about 50% for both devices, while the gain is about 10 dB, and 5 dB for the driver and power transistor, respectively. On the contrary, class A condition provides the highest linearity and the lowest PAE. Notably, the IM3 phase varies from positive to negative values depending on both the class of operation (gate bias voltage) and input power level. The highest efficiency gate bias points of the power stage that achieve $G > 10$ dB and $PAE > 40\%$ are named $\{\bar{X}\}$, and the selected points are $(-1.7, -1.9, -2.1)$.The output power thresholds used to define this constrained subset $\{\bar{X}\}$ (and similarly $\{\bar{Y}\}$ in Eq. 10) were deliberately set higher than the final required output power to account for estimated passive losses of ∼1 dB. This ensures that the combined transistor power exceeds 34 dBm to reliably meet the final target of $P_{\text{out,total}} > 33$ dBm including losses. The best gate biases of M_B and M_D are computed after calculating the variance of the power stage (12). The next step is to generate and sort the $\{Z\}$ set. It includes the gate bias pair combination of M_B and M_D with relative linearity/efficiency parameters such as PAE, Gain, and $\sigma_{IM3,PA}$ for the parallel configuration. Consequently, the best pair bias for power stages M_B and M_D that obtains high linearity improvement is achieved at gate biases $V_{gs_B} = -1.9$V and $V_{gs_D} = -1.7$V. Concerning the driver stages, the gate bias of each transistor (M_A and M_C) is determined based on (13) and (14) to obtain lower linearity values for the series path $IM3_{AB}$, i.e., M_A and M_B, and $IM3_{CD}$, i.e., M_C and M_D. As a result, the best gate bias voltages of dataset $\{D\}$ that achieve the required design goal of high efficiency and linearity meeting the PA parameters; $G_{total} > 20$, $PAE_{total} > 40$, and $P_{out,total} > 2-$W, and $\sigma_{IM3,PA}$, are $V_{gsA} = -1.7$, $V_{gsB} = -1.9$, $V_{gsC} = -1.9$, and $V_{gsD} = -1.7$.

B. SIMULATION AND PERFORMANCE OF THE 2-W PA

The proposed methodology is applied to design a 2−W PA operating within the 10.4-10.8 GHz frequency range. The gate bias voltages are as concluded in the previous section, with all drain voltages set to $V_{DD} = 28$ V. Referring to Fig. 6, the input and output matching networks of each stage of the PA are designed based on the optimal impedances present in the corresponding data set, i.e., $\{X\}$ for the driver stage and $\{Y\}$ power stage. First of all, to ensure unconditional stability, a dedicated stabilization network was implemented at each gate terminal. This network consists of a parallel R–C circuit and a series L–R circuit connected in series and in parallel to the gate terminal, respectively. The L–R branch, in which the inductance is realized as a short transmission line, also serves to provide the gate bias voltage, integrating stabilization and DC feed in a compact layout. The matching networks were designed not only for impedance matching transformation but also to minimize insertion loss. The input matching network ($M_{in,A}$/ $M_{in,C}$) for the driver transistors (M_A/M_C) employs a modified L-network, consisting of a

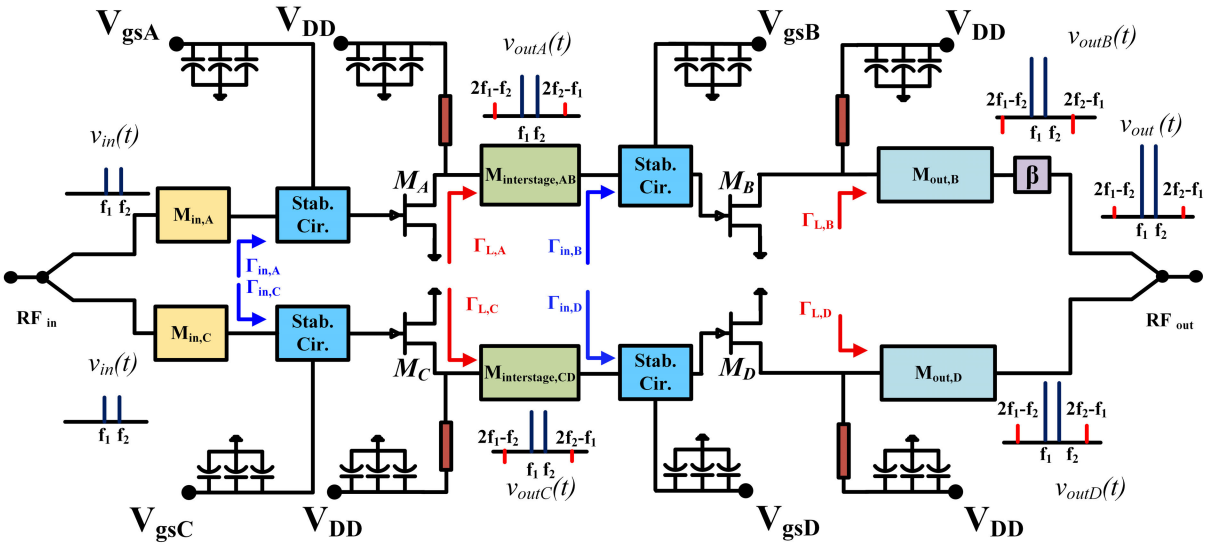


FIGURE 6. Complete circuit schematic of the implemented 2-W MMIC power amplifier, including stabilization, matching networks, and the power combiner.

MIM capacitor, a series microstrip line, and a shunt short-circuited stub. This network transforms the input reflection coefficient of the stabilized device ($\Gamma_{in,A}/\Gamma_{in,C} = 0.27 \angle -110°$) to the 100 Ω characteristic impedance of the divider.

The interstage matching network of the proposed design ($M_{interstage,AB}/M_{interstage,CD}$) (between drivers M_A/M_C and power devices M_B/M_D) is implemented as a Pi-network using open/short stubs, a microstrip line, and a MIM capacitor. It also integrates the drain bias of the driver transistor, transforming the input reflection coefficient of the power transistor ($\Gamma_{in,B}/\Gamma_{in,D} = 0.55\angle -96°$) into the optimum load for the driver one i.e., ($\Gamma_{L,A}/\Gamma_{L,C} = 0.72\angle 25°$).

The output matching network ($M_{out,B}/M_{out,D}$) of the power transistors (M_B/M_D) consists of a Pi-network with a short stub and shunt MIM capacitor. This transforms the 100 Ω combiner impedance to the optimal reflection coefficient ($\Gamma_{L,B}/\Gamma_{L,D} = 0.78\angle 32°$).

After that, the two arms are combined, and the overall PA is evaluated by small-signal and HB simulations. The small-signal simulation results are shown in Fig. 7. Input and output reflection coefficients are lower than −10 dB, with a small-signal gain S_{21} of 21 dB in the entire bandwidth from 10 to 11 GHz.

The large signal simulation results are illustrated in Fig. 8. The power gain of the PA is more than 21 dB, while output power and PAE are higher than 34 dBm and 42%, respectively, over the entire band 10.4 to 10.8 GHz.

The AM-AM shows that the amplitude imbalance is less than ±0.2, as depicted in Fig. 9, whereas AM-PM, shown in Fig. 10, demonstrates a very flat behavior. These results highlight how the selected combination of driver and power stage biasing conditions leads to quite good efficiency and linearity performance at the PA level. The two-tone HB simulation is conducted with a spacing frequency of 10 MHz

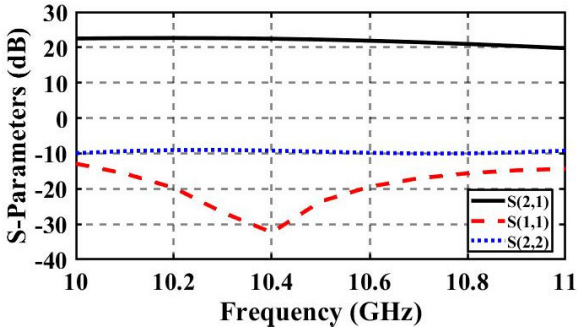


FIGURE 7. Simulated S-parameters of the PA.

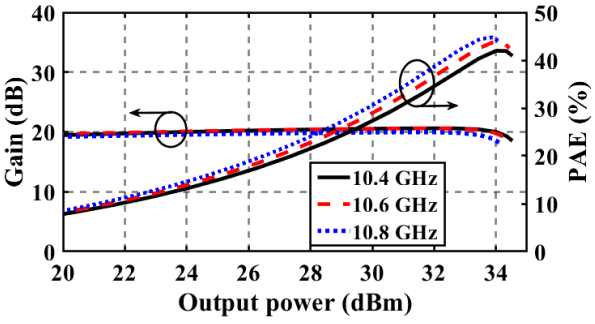


FIGURE 8. Simulated gain and PAE of the PA as functions of the output power.

at different center frequencies from 10.4 to 10.8 GHz and a step of 0.2 GHz, as shown in Fig. 11, demonstrating the PA's optimized IM3 cancellation at back-off (i.e., 30 dBm), where high-PAPR signals typically operate. While saturation (34 dBm) shows expected IM3 degradation to −15 dBc, this represents a deliberate design compromise to maintain 40% PAE at peak power, as most systems spend.

To quantify the effectiveness of IM3 cancellation with a spacing frequency of 10 MHz at center frequency 10.6 GHz,

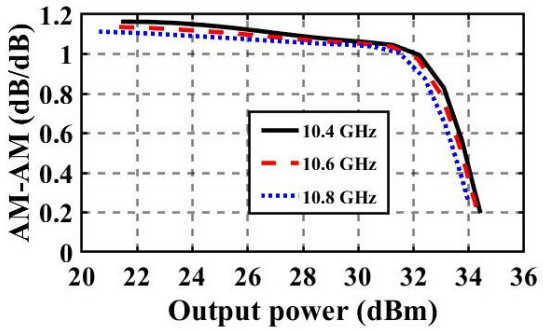


FIGURE 9. AM-AM of the PA as a function of the output power.

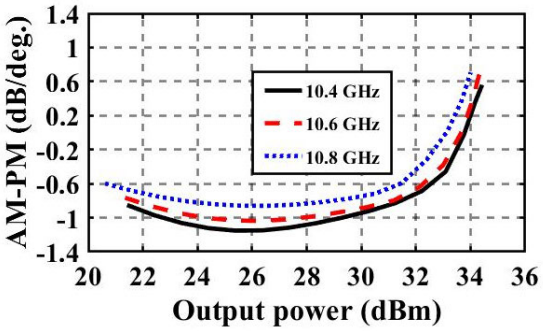


FIGURE 10. AM-PM of the PA as a function of the output power.

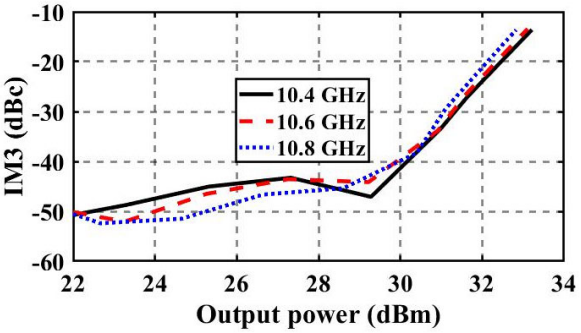


FIGURE 11. IM3 of the PA as a function of the output power.

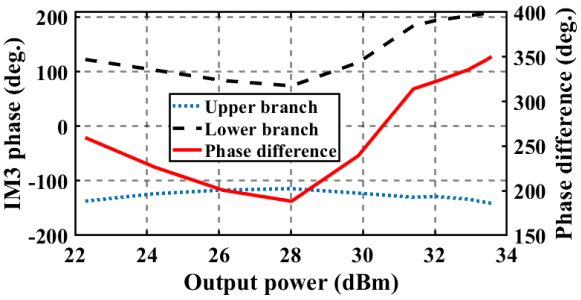


FIGURE 12. Phase characteristics of IM3 components at mid band: Upper/Lower branch and the phase difference between the two branches.

phase analysis in Fig. 12 confirms a consistent phase difference of less than 240° between branches, with near-ideal 180° cancellation occurring precisely at our targeted operating point of lower than 30 dBm. This cancellation is achieved

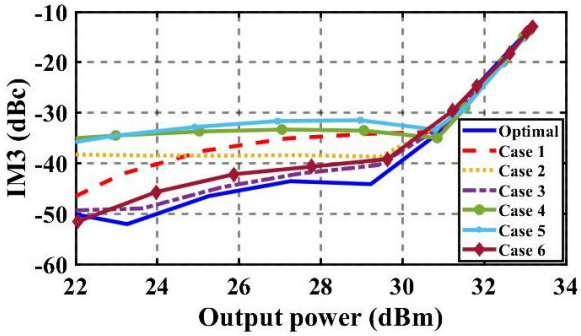


FIGURE 13. Simulation of IM3 levels versus output power for the optimal bias combination and six suboptimal cases.

TABLE 1. Performance comparison of bias combinations.

Case	Bias condition (V)	IM3 @ 30dBm (dBc)
Optimal	-1.7/-1.9/-1.9/-1.7	-40
Case 1	-1.7/-1.9/-1.7/-1.9	-35
Case 2	-1.9/-1.7/-1.9/-1.7	-38
Case 3	-1.9/-1.7/-1.7/-1.7	-38
Case 4	-1.9/-1.9/-1.7/-1.9	-35
Case 5	-1.9/-1.7/-1.9/-1.9	-32
Case 6	-1.7/-1.7/-1.7/-1.9	-38

by optimally biasing the driver stages (M_A/M_C) and power stages (M_B/M_D) to produce opposite IM3 phases ($\approx 90°$ and $\approx -90°$ respectively), enabling vector summation that suppresses third-order distortion by > 15 dBc. In addition, Fig. 13 compares the optimal bias combination ($V_{gsA} = -1.7$ V, $V_{gsB} = -1.9$ V, $V_{gsC} = -1.9$ V, $V_{gsD} = -1.7$ V) against six alternative cases. The optimal case achieves IM3 suppression of -40 dBc up to 30 dBm output power, i.e., 8 dB improvement over non-optimized biases (e.g., Cases 1–6). This improvement could be up to 15 dB for lower output power at 24 dBm. Table 1 compares the linearity performance of the proposed GaN PA under different gate bias combinations. Suboptimal cases (Cases 1–6) show degraded performance, with IM3 levels ranging from -32 to -38 dBc at an output power of 30 dBm rather than the optimal gate bias selected by the proposed algorithm IM3 level -40 dBc. To quantify the improvement over a traditional biasing scheme, where all transistors are biased identically, we compare our optimal case against symmetric biasing. When all four transistors are biased at the high-efficiency point of $V_{gs} = -1.9$ V, the IM3 level degrades to -32 dBc at 30 dBm output power. Similarly, biasing all transistors at $V_{gs} = -1.7$ V yields -35 dBc. Our optimized asymmetric biasing scheme achieves -40 dBc, representing a **5–8** dB improvement in linearity while maintaining high PAE. This demonstrates the ability of the algorithm to identify the best gate bias voltages that simultaneously maximize linearity and efficiency.

IV. EXPERIMENTAL RESULTS

The fabricated monolithic microwave integrated circuit (MMIC) power amplifier, shown in Fig. 14, represents the

physical realization of the proposed series-parallel GaN PA architecture discussed in previous sections. Manufactured using WIN Semiconductors $0.15-\mu$m GaN-on-SiC process, the amplifier occupies a compact $3.7\times3.3\ mm^2$ die area while delivering good performance in the X-band frequency range (10.4-10.8 GHz). This section details the small-signal characterization and large-signal performance of the PA under both continuous-wave and two-tone excitation, demonstrating its compliance with 6 G communication system requirements.

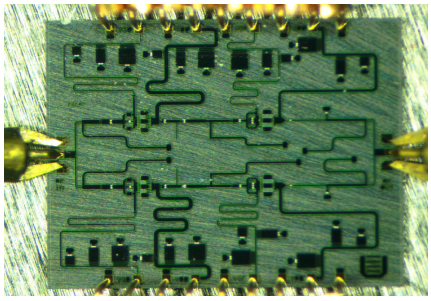


FIGURE 14. Fabricated MMIC microscopic photograph.

A. CONTINUOUS WAVE SIGNAL MEASUREMENT

The proposed PA was measured in small-signal condition over the entire band, from 10.4 to 10.8GHz, at the following bias conditions: drain voltage for drivers and power stages of 28 V, and gate biases of $\{V_{gs_A},V_{gs_B},V_{gs_C},V_{gs_D}\} = \{-1.7,-1.9,-1.9,-1.7\}$V and $\{I_{ds_A},I_{ds_B},I_{ds_C},I_{ds_D}\} = \{4.5, 6, 4, 7\}$mA, respectively. The small signal measurement results are shown in Fig. 15. A flat gain of about $S_{21} = 21$ dB is registered with input and output return losses from 10 GHz to 11 GHz better than 10 dB and good matching between the S-parameters measurement and simulation.

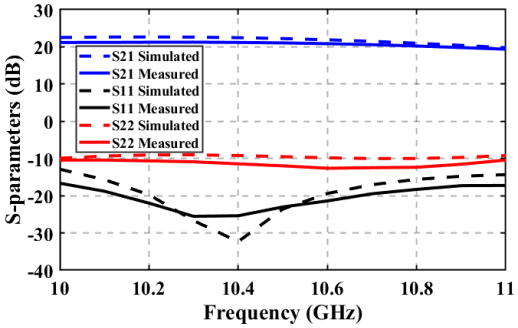


FIGURE 15. S-parameters simulation and measurement of the proposed PA.

The large signal one-tone measurements are shown in Fig. 16. The power gain is higher than 19 dB with the gain flatness better than 0.5dB. The output power is higher than 34dBm with an associated PAE ranging between 37% and 40% over the bandwidth. The simulated saturated output power of 34.5 dBm and peak PAE of 42% (Fig. 8) are in close agreement with the measured values of 34 dBm and 40% (Fig. 16), respectively. The minor discrepancy of less than

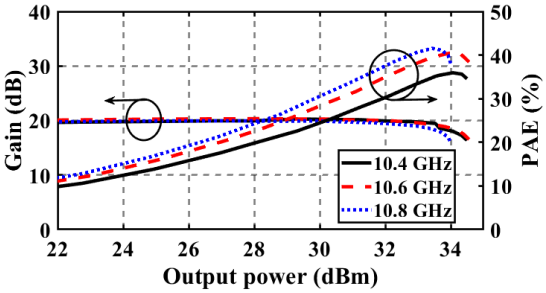


FIGURE 16. Power gain and PAE measurement results.

0.5 dB in output power is attributed to the estimated passive losses on the on-chip matching networks and combiner.

B. TWO-TONE SIGNAL MEASUREMENTS

The two-tone measurements are performed at the center frequency of 10.6GHz with different tone-spacings of about 10MHz, 50MHz, 100MHz, and 200MHz. The power gain is about 19dB, and the 1-dB compression point occurs at an output power of 32.2 dBm, while the saturated output power is about 33.5 dBm with a PAE of more than 37%, as shown in Fig. 17.

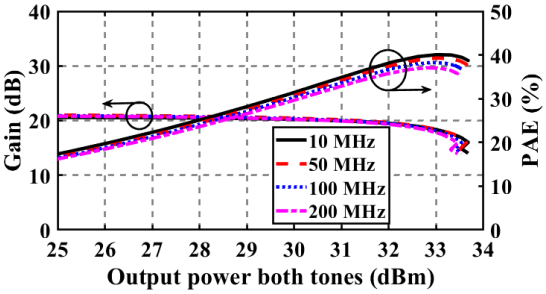


FIGURE 17. Measured two-tone power gain and PAE with different tone spacing.

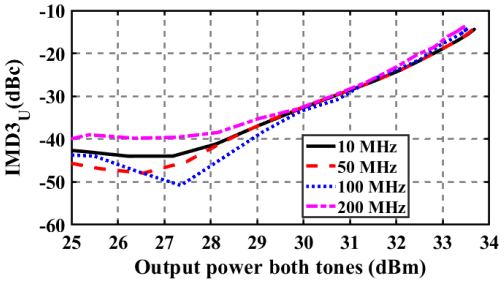


FIGURE 18. Measured upper IM3 at center frequency 10.6 GHz with different spacing (10-200) MHz.

Fig. 18 and Fig. 19 show the upper and lower IMD3 versus total output power, respectively. The resulting C/I is lower than 30dBc for an output power up to 30dBm with a corresponding PAE of more than 33%. The critical IM3 cancellation behavior, which determines the observed linearity improvement, is accurately predicted by the simulation in Fig. 13. The measured results in Fig. 18 confirm

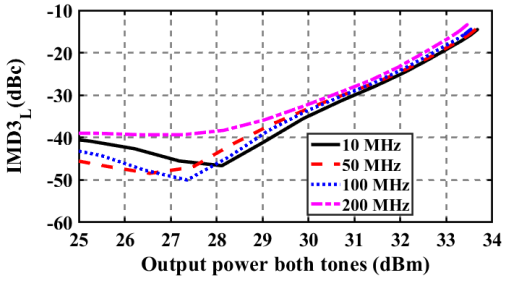


FIGURE 19. Measured lower IM3 at center frequency 10.6 GHz with different spacing (10-200) MHz.

the deep IM3 cancellation near 30 dBm output power. The simulated and measured IM3 levels at this point are −38 dBc and −35 dBc, respectively, demonstrating the model's high fidelity in predicting this high-order nonlinear effect.

C. MODULATED SIGNAL MEASUREMENT

To evaluate the MMIC RF PA performance under realistic operating conditions, large-signal modulated characterization was performed using a standardized 3GPP WCDMA signal. The test signal was a WCDMA QPSK waveform with a symbol rate of 3.84 Msps and bandwidth 5 MHz, exhibiting a peak-to-average power ratio (PAPR) of 3.5 dB. This analysis focuses on two critical metrics for modern communication systems: out-of-band spectral regrowth, quantified by the Adjacent Channel Power Ratio (ACPR), and in-band distortion, measured by the Error Vector Magnitude (EVM).

The measured ACPR for the upper and lower adjacent channels (with an offset of 5 MHz) at the center frequency 10.6 GHz and the ACPR is approximately −27 dBc at the output power of 33.2 dBm as shown Fig. 20 with an average PAE of more than 35% and an average gain of about 19 dB as shown in Fig. 21. Fig. 22 depicts the normalized spectral density at different power levels 6-dB OBO, 3-dB OBO, and Psat at 33.2 dBm, respectively.

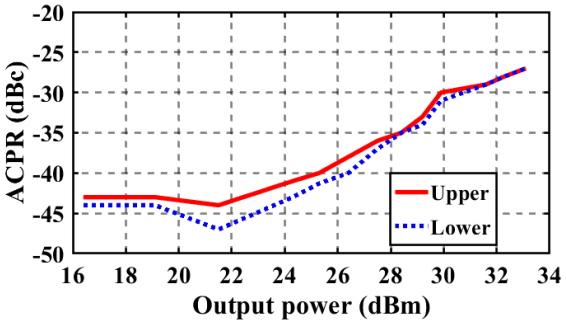


FIGURE 20. Lower and upper ACPR versus average output power for the MMIC at center frequency 10.6 GHz.

For the proposed PA, EVM measurements were conducted across various output power levels at center frequency 10.6 GHz as shown in Fig. 23. At 6-dB OBO, the EVM measured 1.9%, demonstrating excellent linearity suitable for high-order modulation schemes. As the output power

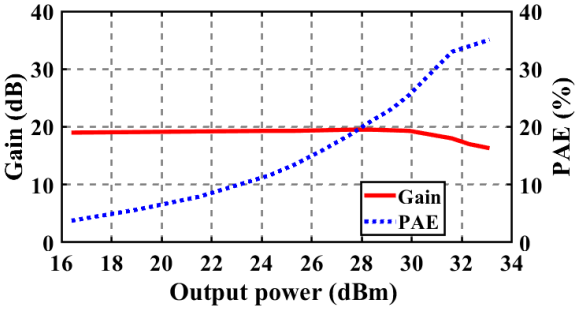


FIGURE 21. Measured average gain and PAE versus average output power at 10.6 GHz.

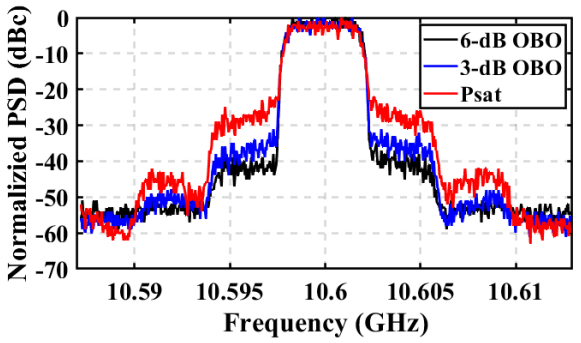


FIGURE 22. Normalized power spectral density of 5MHz WCDMA signal at different average output power levels at center frequency 10.6 GHz.

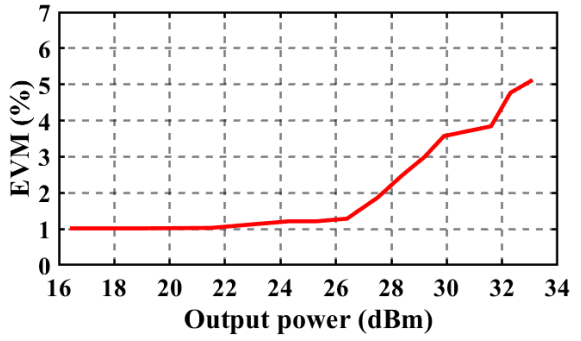


FIGURE 23. Measured average EVM versus output power.

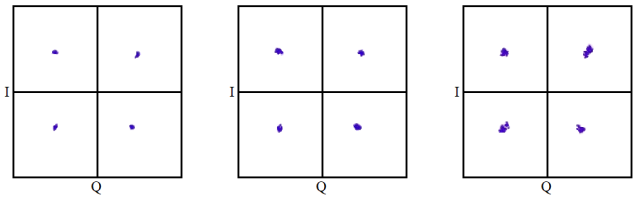
increased to 3-dB OBO, the EVM degraded to 3.7%. At saturation power, the EVM increased to 5.1%, which remains within acceptable limits for QPSK modulation. The measured EVM results demonstrate a degradation with increasing output power, maintaining compliance with the stringent linearity requirements for modern communication standards even near saturation. This performance highlights the effectiveness of the proposed linearization techniques and bias optimization methodology in maintaining signal fidelity across the operating power range.

The constellation diagrams in Fig. 24 provide visual confirmation of the PA's linearity performance at different power levels. At 6-dB OBO (Fig. 24a), the constellation points exhibit minimal spreading, corresponding to the excellent 1.9% EVM measurement. The clear separation between symbol states indicates minimal distortion and noise

TABLE 2. Comparison between the fabricated MMIC and the state of the art PAs.

Ref.	CW signal								Modulated signal			
	GaN Process (μm)	Freq. (GHz)	Gain (dB)	PAE (%)	FoM[a] (%)	Psat (dBm)	OP1dB (dB)	IM3 (dBc)	BW (MHz)/ PAPR (dB)	ACPR (dBc)/ P_{avg} (dBm)	PAE (%)	Gain (dB)
[24] 2021	0.15	9.5-10.5	21	36.51	64	35.6	33.5	-10	100/7.9	-27	30.2	21
[25] 2020	0.15	9.7	20	50	88.2	40	37	–	20/7	-22/33	34	20
[26] 2024	0.15	9.1-10.3	17	36-40.7	62.5-72.9	43.5-44.5	35	–	–	–	–	–
[27] 2017	0.25	8.5-10.5	24	35-37	59.7-66.6	43.2-44.7	40	–	–	–	–	–
[28] 2025	0.15	10-16	19-17	34.6-45.9	69.2-90.3	35.1-36.7	32	–	122.88/7.12	-28.2/ 31.4	28	19
[29] 2025	0.12	9.6-10.4	10	40-35	70.4-62.8	36.6	34.5	–	10/6	-30/ 31.9	27	10
This work	0.15	10.4-10.8	19	36-41	65-74.5	33.9	33.7	-15	5/3.5	-30/31	33	19

$$\text{FoM}^{a} = \text{PAE} \cdot (\text{Freq GHz})^{0.25}$$



(a) (b) (c)

FIGURE 24. Constellation diagrams of the proposed PA at center frequency 10.6 GHz (a) 6 dB OBO (b) 3 dB OBO (c) saturated output power.

impact. At 3-dB OBO (Fig. 24b), increased spreading is observable around the constellation points, consistent with the degraded 3.7% EVM, but the symbol decision boundaries remain well-defined. At saturation power (Fig. 24c), further spreading occurs due to increased nonlinear distortion, yet the constellation maintains its structural integrity with the 5.1% EVM remaining within acceptable limits for QPSK modulation. These visual results correlate well with the quantitative EVM measurements and demonstrate the PA ability to maintain signal quality across its operating range.

Comparing simulations and measurements, a very good agreement is achieved. A comprehensive comparison between the proposed PA and state-of-the-art designs is presented in Table 2, highlighting significant improvements in both CW and modulated performance metrics. The proposed PA achieves competitive performance, with a peak PAE of 40% and superior linearity (IM3 < -30 dBc at 33% PAE), outperforming prior works such as [24] (-15 dBc vs. -10dBc). Similarly, [26] and [27] report higher Psat ($43.5 - 44.7$ dBm) but lack the nonlinearity since OP1dB is less than Psat by at least 5 dB, highlighting our balanced trade-off between power, efficiency, and distortion.

Under modulated operation, our design demonstrates exceptional performance with an ACPR of -30 dBc at 31 dBm average output power, representing a 3 dB improvement over [24] (-27 dBc) and comparable to the state-of-the-art [29] while operating with higher PAE (33% vs. 27%). The achieved FoM range of 65-74.5% is highly competitive, particularly considering the excellent linearity maintained across the 10.4-10.8 GHz frequency band.

These results validate the proposed design methodology, which combines analytical IM3 cancellation (Section II) with systematic gate-bias optimization (Fig. 2) to achieve first-pass success. The measured performance (IMD3 ≤ -15 dBc, PAE $> 36\%$ across 10.4 GHz to 10.8 GHz) and ACPR of -30 dBc, EVM of 1.9-5.1% across different back-off levels at center frequency 10.6 GHz demonstrates that the series-parallel topology and the developed algorithm for optimal bias selection effectively eliminate iterative tuning while maintaining robust linearity-efficiency trade-offs. This balanced performance approach is particularly advantageous for 6 G systems requiring both high efficiency and exceptional spectral purity for advanced modulation schemes.

V. CONCLUSION

This paper demonstrates a systematic approach for designing high-efficiency GaN power amplifiers with enhanced linearity through an optimized series-parallel configuration, supported by a novel algorithm for determining optimal gate bias conditions. The proposed algorithm eliminates traditional trial and error methods while achieving state-of-the-art performance in both efficiency and linearity. The methodology proves particularly valuable for 6G communication systems that demand stringent linearity requirements without compromising power-added efficiency. The proposed design comprises two parallel PA branches, each consisting of a driver and power stage in a series configuration. The analytical fundamental output voltage and the total third intermodulation distortion expressions of the series-parallel PA are derived. Moreover, the proposed algorithm has been provided to determine the best combination of gate bias for drivers and power stages to achieve high linearity and efficiency in the PA. Based on the analysis and detailed simulation results, 2-W high linear and efficient series-parallel MMIC RF PA for the 400 MHz bandwidth at

center frequency 10.6 GHz is fabricated on a $0.15-\mu$m GaN-on-SiC process. The fabricated amplifier exhibited a power gain of 19 dB, a saturated output power of 34 dBm, a PAE of 40%, and a 1-dB output compression point at 33.5 dBm. When the IMD3 of the proposed design reaches −30 dBc, its PAE is more than 33% for the lower and upper IMD3, and the output power is 30dBm. Under modulated 5 MHz WCDMA excitation, the amplifier maintained an ACPR of approximately −30 dBc and an EVM as low as 3.9 % at average output power 31 dBm, validating its ability to handle modern complex waveforms with high fidelity. It achieves competitive results as compared to other published works, which verifies the proposed methodology and makes it an excellent candidate for modern communication systems.

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