Observation of 2D Conduction in Ultrathin Germanium Arsenide Field-Effect Transistors

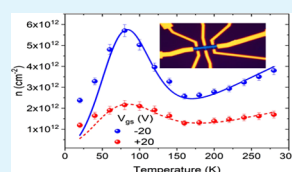Alessandro Grillo, Antonio Di Bartolomeo,* Francesca Urban, Maurizio Passacantando, Jose M. Caridad, Jianbo Sun, and Luca Camilli*
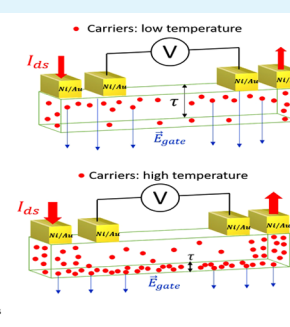
ACCESS | Metrics & More | Article Recommendations

ABSTRACT: We report the fabrication and electrical characterization of germanium arsenide (GeAs) field-effect transistors with ultrathin channels. The electrical transport is investigated in the 20−280 K temperature range, revealing that the p-type electrical conductivity and the field-effect mobility are growing functions of temperature. An unexpected peak is observed in the temperature dependence of the carrier density per area at ∼75 K. Such a feature is explained considering that the increased carrier concentration at higher temperatures and the vertical band bending combined with the gate field lead to the formation of a two-dimensional (2D) conducting channel, limited to few interfacial GeAs layers, which dominates the channel conductance. The conductivity follows the variable-range hopping model at low temperatures and becomes the band-type at higher temperatures when the 2D channel is formed. The formation of the 2D channel is validated through a numerical simulation that shows excellent agreement with the experimental data.

➢ Areal carrier density $n(T)$ in few-layer **GeAs** shows a broad peak ∼75 K.

➢ A highly conductive 2D channel close to the dielectric interface, which screens the gate field, is formed at T>100 K.

➢ A model based on temperature-dependent channel thickness $\tau(T)$ explains the experimental data.

KEYWORDS: germanium arsenide, 2D conduction, temperature-dependent conduction, field-effect transistors, carrier density, mobility, variable-range hopping

INTRODUCTION

Since the isolation of graphene,[1] there has been growing interest in the research of new two-dimensional (2D) materials for the realization of next-generation electronic devices.[2,3] Several transition metal dichalcogenides (TMDs) have promptly emerged as possible substitutes or complements to graphene[4] and have already been investigated and proposed for several applications.[5−13] More recently, the search for new types of 2D materials has led to the investigation of binary compounds of IV and V groups. Indeed, theoretical calculations have indicated that MX compounds, with M = Si, Ge, Sn, or Pb and X = P, As, Sb, or Bi, might have crystalline layered structures with orthorhombic ($Cmc2_1$ for SiP and $Pbam$ for SiP_2 and $GeAs_2$) or monoclinic ($C2/m$ for GeP, GeAs, and SiAs) symmetries.[14−17] Several studies have investigated the band gap,[18] lattice structure,[14] thermoelectric performances,[19] and the Hall mobility[20] of such materials as bulk crystals, but there have been only a few reports on their electrical properties in the form of ultrathin or monolayer flakes.[21,22]

Among the IV−V compounds, GeAs has attracted attention for possible optoelectronic applications and for its high in-plane anisotropy.[21,22] GeAs bulk crystalizes in a layered structure, in the space group $C2/m$, in which each Ge atom is bonded to one Ge atom and three As atoms forming distorted $As_6@Ge_2$ octahedra.[23] GeAs layers, terminated by As atoms, are kept together by weak van der Waals forces and show two different types of Ge−Ge bonds. One type is parallel and the other one is perpendicular to the layer plane, highlighting the anisotropic nature of the GeAs crystal structure (see Figure 1a). Similar to TMDs, the GeAs band gap changes according to the number of layers. Numerical calculations and optical band gap measurements indicate that germanium arsenide indirect band gap ranges from ∼0.57 to 0.65 eV for the bulk[19,20] to 1.6−2.1 eV for the monolayer.[24,25]

In this work, we report the electrical characterization of GeAs back-gate field-effect transistors fabricated using exfoliated flakes of 12 nm thickness. We measure the output and transfer characteristics in a four-probe configuration, highlighting the p-type nature of the GeAs flakes in a vacuum. We investigate the temperature behavior of the transistors in a
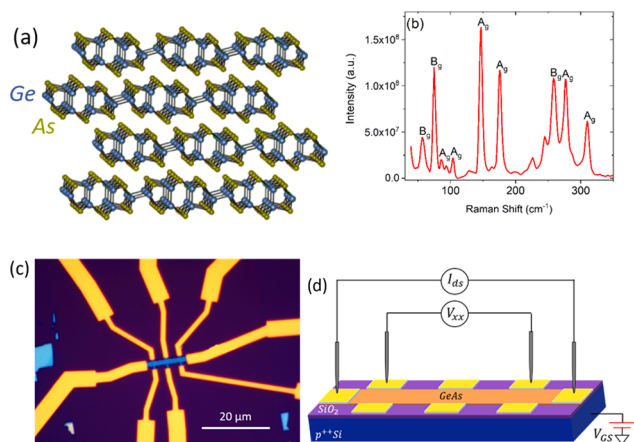
Figure 1. (a) Atom arrangement in GeAs layers. (b) Raman spectrum of a GeAs flake. (c) Optical image of the Hall bar device with Ni/Au electrodes. (d) Four-probe measurement setup.

range from 20 to 280 K, estimating figures of merit such as channel resistivity and field-effect mobility. The free carrier density per area, studied as a function of temperature, shows an unexpected broad peak at around 75 K. To explain this anomaly, we propose a model based on the modulation of the channel thickness with temperature. At low temperatures, the intrinsic carrier concentration in the channel is limited and the electric field of the gate controls the whole thickness of the GeAs flake. At higher temperatures, the increased carrier injection from the contacts and ionization of defects enable the formation of a 2D highly conductive channel close to the dielectric interface, which screens the gate field and confines it to the first few layers of the material. Such a model is corroborated by the estimation of an ~0.4 nm Debye screening length at room temperature. We compare the numerical simulation of the model with the experimental data obtaining an excellent agreement. To account for the temperature behavior of the resistivity, we use the variable-range hopping (VRH) model at lower temperatures and the thermally

activated band-conduction mechanism at higher temperatures. We find that at lower temperatures, the GeAs flake behaves like a three-dimensional system in which the main conduction mechanism is hopping among intragap states, while at higher temperatures, after the formation of the 2D channel, the conduction is dominated by thermal activation of carriers (holes) to the valence band, which leads to the band-type conduction regime.

■ MATERIALS AND METHODS

Ultrathin GeAs flakes were exfoliated from bulk GeAs single crystals using a standard mechanical exfoliation method by adhesive tape. The flakes were transferred onto degenerately doped p-type silicon substrates, covered by 300 nm-thick SiO_2, on which they were located through optical microscopy. The Raman spectrum of a flake (Figure 1b) was measured under an excitation line of 455 nm by a Thermo Scientific DXR microscope and, in agreement with other studies,[26] it displays six Raman A_g modes at 94, 105, 147, 174, 276, and 308 cm^{-1} and three Raman B_g modes at 58, 76, and 257 cm^{-1}. By means of an atomic force microscope (AFM), we selected a flake of ~12 nm thickness, corresponding to about 20 layers, on which we performed standard electron-beam lithography, realizing a typical Hall bar structure, intentionally oriented along one of the crystallographic axes of the material. We then used electron-beam evaporation to deposit 5 nm Ni/40 nm Au as electrodes (Figure 1c). A back-gate contact was formed covering the scratched area of the Si substrate with silver paste.

Electrical measurements were carried out in an Oxford Instrument Teslatron PT cryostat electrically connected with a semiconductor parameter analyzer to perform the standard four-probe characterization of the devices (Figure 1d). All of the measurements were carried out at a pressure of ~10^{-5} mbar within the temperature range from 20 to 280 K.

■ RESULTS AND DISCUSSION

We show in Figure 2 the electrical characterization of the GeAs transistor at room temperature. The output characteristics, i.e., the drain−source current (I_{ds}) as a function of the voltage drop between two inner contacts (V_{xx}) with the gate-source voltage (V_{gs}) as a control parameter, exhibit linear behavior. The
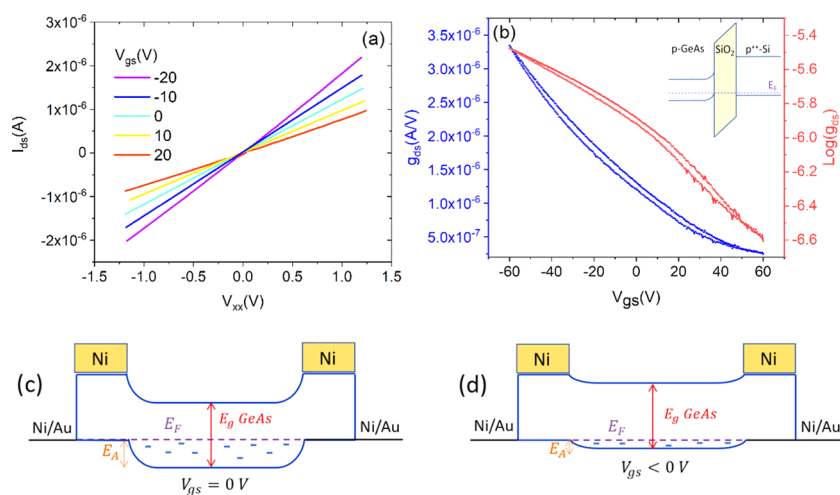
Figure 2. (a) Output characteristic recorded in the four-probe configuration with the V_{gs} bias being between −20 and 20 V. (b) Transfer characteristic recorded in the four-probe configuration showed both on linear and logarithmic scales. The inset shows the band diagram in the vertical direction at zero bias clarifying that the device is a normally-on transistor. (c, d) Band diagram along the channel (horizontal) direction, showing alignment between Ni/Au contacts and GeAs at $V_{gs} = 0$ and $V_{gs} < 0$, respectively. The small blue dashes represent the (mostly empty) trap states for holes. The contact region is more doped than the channel (not on scale), thus giving rise to an energy barrier E_A, which is modulated by the gate.
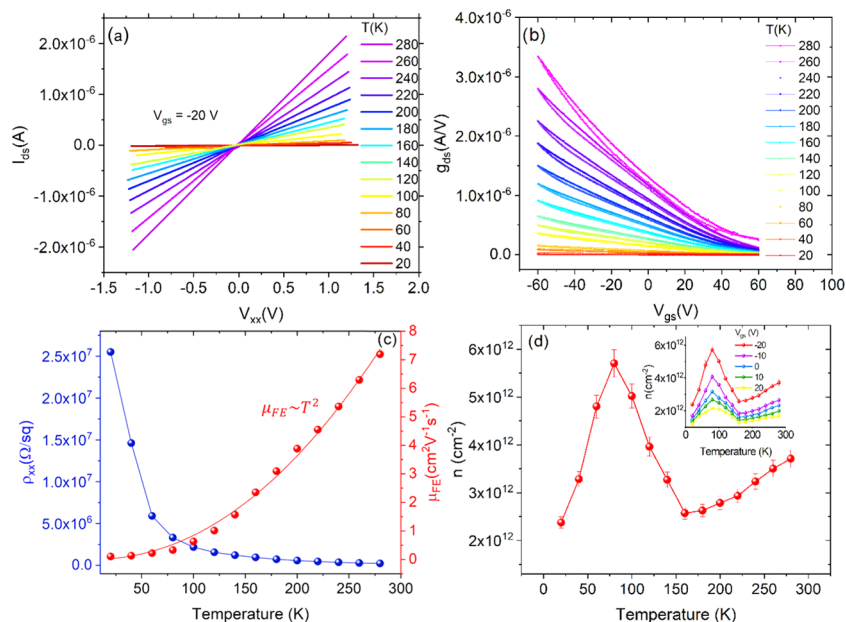
Figure 3. (a) I_{ds} versus V_{xx} curves at different temperatures. (b) Transfer characteristics recorded for a loop of the voltage bias at different temperatures. (c) Channel resistivity (blue dots) and field-effect mobility (red dots) as a function of temperature. The superposed red line is the quadratic fit. (d) Carrier density n versus temperature at $V_{GS} = -20$ V. The inset shows n as a function of temperature at several gate biases. The uncertainties are obtained from the standard error propagation.

application of the gate voltage affects the overall conductance of the sample without modifying the $I_{ds}-V_{xx}$ linearity as expected for four-probe measurements that exclude the effect of the contact resistance.[27−29] The transfer characteristic, i.e., the $g_{ds}-V_{gs}$ curve ($g_{ds} = I_{ds}/V_{xx}$ is the channel conductance) measured over a loop of the gate voltage is reported in Figure 2b. It shows a typical p-type behavior with a modulation that is less than 1 order of magnitude. We did not reach the off-state of the transistor in the applied voltage range, which was limited to avoid the breaking of the device gate dielectric. The p-type behavior is favored by the low work function[15] of GeAs (~4 eV) and the higher work function of the degenerate p-Si gate (>5.12 eV) that cause the vertical band alignment shown in the inset of Figure 2b. Furthermore, the Ni Fermi level (work function of 5.15 eV) tends to align below the valence band of GeAs, resulting in ohmic contacts. Furthermore, intrinsic defects such as Ge vacancies, the interaction with the SiO$_2$ gate dielectric, and the oxidation of the topmost layers of the flake would act as p-type dopants in the material and provide intragap states.[14,15] Hole injection from the metal leads makes the area below and near the contacts more doped than the rest of the long channel, thereby giving rise to an energy barrier E_A, which can be modulated by the gate (see Figure 2c,d).[30]

Differently from few-layer TMD-based transistors,[31−35] the transfer characteristic exhibits negligible hysteresis indicating limited charge trapping during a gate voltage loop.

The temperature dependence of the electric behavior of the device is investigated in Figure 3. We measured the output and transfer characteristics every 20 K in the 20−280 K temperature range (Figure 3a,b). We found a decreasing current and conductance with lowering temperature without any other apparent change in the behavior of the device. From the linear fit of the $I_{ds}-V_{xx}$ curves, recorded at $V_{gs} = -20$ V, we estimated the resistivity ρ of the sample as a function of the temperature ($\rho = \frac{RW}{L}$, where R is the resistance evaluated from the fit, and $L = 6$ and $W = 2.7$ μm are the channel length and

width, respectively). Figure 3c shows a decreasing ρ for increasing temperature, typical of a semiconducting material.

Using the transfer characteristics, considering their nonlinear behavior, we expressed the field-effect transistor (FET) channel conductance as

$$g_{ds} = \frac{I_{ds}}{V_{xx}} = \frac{W}{L}\mu_{FE}C_{ox}|V_{gs} - V_{th}|^{\alpha} \tag{1}$$

where μ_{FE} is the field-effect mobility; $C_{ox} = \frac{\epsilon_0 \cdot \epsilon_{SiO_2}}{t_{SiO_2}} = 1.15 \times 10^{-8}$ (F/cm^2) is the capacitance per unit area of the gate dielectric, where $\epsilon_0 = 8.85 \times 10^{-14}$ F/cm, $\epsilon_{SiO_2} = 3.9$, and $t_{SiO_2} = 300$ nm are the vacuum permittivity, the SiO$_2$ relative permittivity, and thickness, respectively; V_{th} is the threshold voltage; and $\alpha \geq 1$ is a dimensionless parameter that accounts for a possible V_{gs}—dependence of mobility.[31] According to eq 1, when the $I_{ds}-V_{gs}$ curve is linear and $\alpha = 1$, the mobility can be obtained as

$$\mu_{FE} = \frac{L}{W}\frac{1}{C_{ox}}\frac{dg_{ds}}{dV_{gs}} \tag{2}$$

To have a fair comparison with the values of ρ obtained from $g_{ds}-V_{xx}$ curves at $V_{gs} = -20$ V, we performed the linear fit of the transfer characteristics in a small interval around $V_{gs} = -20$ V. Figure 3c shows the mobility μ_{FE} as a function of temperature T. The quadratic dependence, $\mu_{FE} \sim T^2$, points toward a mobility dominated by Coulomb scattering due to ionized impurities.[36] Indeed, it is well known that the mobility is affected by two competitive mechanisms, i.e., the ionized impurity scattering and the phonon scattering.[36] The first mechanism dominates at lower temperatures and yields increasing mobility with increasing temperature, while phonon scattering becomes the prevailing mechanism at higher temperatures and causes decreasing mobility. As already mentioned, charged impurities leading to Coulomb scattering
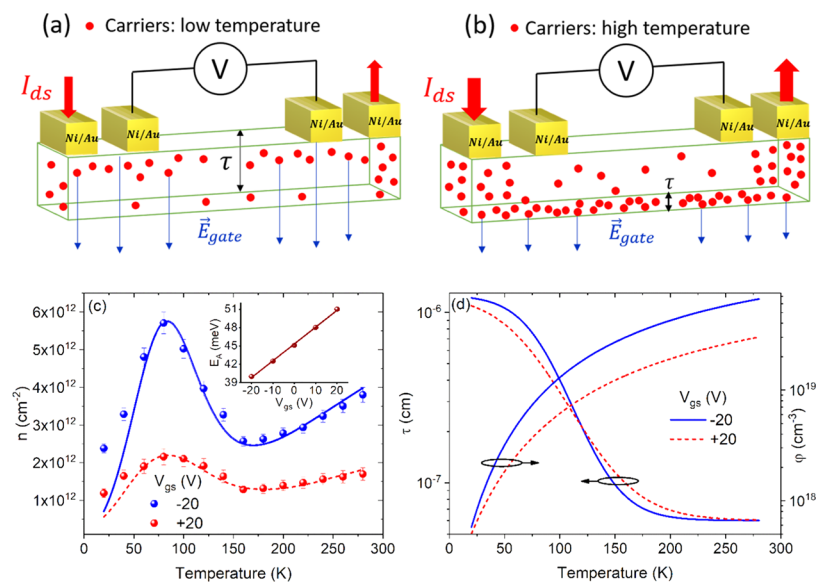
Figure 4. (a) Schematic of the GeAs flake at low temperatures with low carrier density and the electric field of the gate at $V_{GS} < 0$ V (blue arrows) controlling the entire thickness. (b) Schematic of the GeAs flake at high temperatures with the formation of a highly conductive channel confined to a thin interfacial layer, which screens the electric field of the gate (blue arrows). The drawings are not on the scale. (c) Numerical simulation of the 2D carrier density as a function of temperature for $V_{gs} = \mp 20$ V (fitting lines superposed the experimental data). The inset shows E_a as a function of the applied gate potential. (d) Effective thickness of the channel (blue lines) and three-dimensional carrier density (red lines) as a function of temperature for $V_{gs} = \mp 20$ V.

and increasing μ_{FE} are due to the intrinsic defects of GeAs, the SiO$_2$ interface states, and the oxidation of the topmost layers of the flake.

Having computed $\mu_{FE}(T)$ and $\rho(T)$ at each of the considered temperatures, we estimated the carrier density per unit area n (in cm^{-2}) as a function of temperature from the relation

$$n(T) = \frac{1}{q\rho(T)\mu_{FE}(T)} \qquad (3)$$

where q is the electron charge. Figure 3d shows that $n(T)$ exhibits an unexpected and pronounced peak at $T \sim 75$ K, followed by a smoother increase for $T > 150$ K. In a doped three-dimensional semiconductor, the carrier density would show a different temperature behavior.[36] Specifically, an initial rapid increase due to the ionization of dopant atoms by thermal energy (freeze-out region, up to ~150 K for medium-doped Si) would be followed by a plateau over a wide temperature range when complete ionization is reached (extrinsic region, ~150 to 500 K for medium-doped Si) and would finally evolve in an exponential increase at higher temperatures due to the intrinsic generation of electron–hole pairs (intrinsic region).

To explain the reported anomalous behavior, we propose a model that considers a temperature-dependent thickness of the channel in which most of the conduction occurs. The 2D carrier density per unit area can be expressed as $n(T) = \varphi(T)\tau(T)$, where φ is the carrier density per unit volume in cm^{-3} and τ is the thickness of the conducting channel. The current in the GeAs flake is due to the carriers injected from the Ni contacts that overcome the E_A barrier (Figure 2c,d). Therefore, $\varphi(T)$ in the region between the inner contacts (Figure 4a,b) can be expressed as[37]

$$\varphi(T) = A \exp\left[-\frac{E_A}{kT}\right] \qquad (4)$$

where k is the Boltzmann constant, E_A is the barrier between contact and channel regions, and A is a proportionality constant that can be considered as a fitting parameter of the model. At low temperature (<80 K), there is a limited amount of carriers as well as high intralayer resistance that suppresses the vertical transport with respect to the in-plane one.[30,38] In this regime, conduction occurs mainly through the layers in closer contact with the metal leads (especially the topmost ones) and the gate electric field controls the entire flake thickness (Figure 4a). With increasing temperature, defect ionization and injection from the contacts increase. The newly available carriers, pushed by the applied gate voltage and the favorable vertical band bending (see the inset of Figure 2b) toward the interface with the gate dielectric, form a 2D channel, which becomes more and more conductive with increasing temperature. This channel now screens the gate field, and any variation of the gate voltage affects mainly the bottommost layers of the flake. In this regime, the conduction is dominated by few atomic GeAs layers closer to the gate, i.e., the effective conducting thickness $\tau(T)$ controlled by the gate is reduced (Figure 4b).

Such a model is confirmed by the measurement of $n(T)$ at various gate biases, shown in the inset of Figure 3d. Indeed, the 2D channel at the interfacial region between the gate dielectric and the flake is hampered at positive gate voltages by the opposing gate field. Going to positive gate voltages, the 2D conductive channel is gradually suppressed and so is the carrier density n and its peak at ~75 K.

According to the model, with an appropriate choice of $\varphi(T)$ and $\tau(T)$, we computed $n(T)$ and obtained an excellent agreement with the experimental data, as shown in Figure 4c, where we display $n(T)$ at $V_{gs} = -20$ V (continuous blue line) as well as at $V_{gs} = 20$ V (dashed red line). The slight deviation below 50 K could be caused by additional conduction mechanisms occurring at low temperature (such as hopping, see later). The carrier density per volume $\varphi(T)$, given by eq 4,
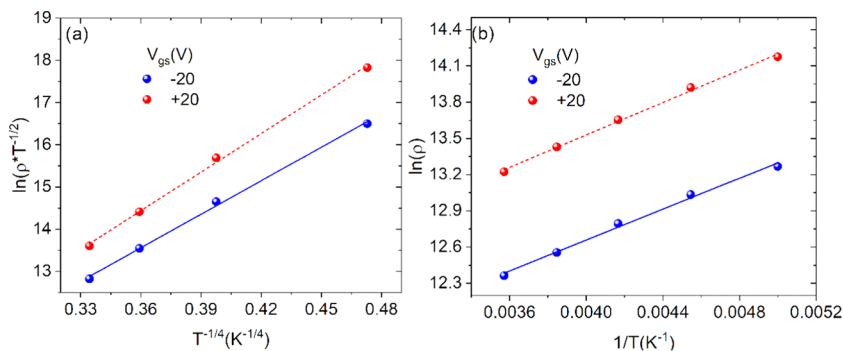
Figure 5. (a) Experimental data and linear fit of $\ln(\rho T^{-1/2})$ at $V_{gs} = \mp 20$ V as a function of $T^{-1/4}$ at low temperature, indicating the three-dimensional nature of the investigated system. (b) Experimental data and linear fit of $\ln(\rho)$ at $V_{gs} = \mp 20$ V as a function of T^{-1} at high temperature, indicating the band conduction regime of the investigated system.

is shown by the red lines of Figure 4d, with E_A being obtained as a fitting parameter and displayed as a function of V_{gs} in the inset of Figure 4c. For $\tau(T)$, we used a steplike function, $\tau(T) = \frac{A}{1 + \exp(BT)} + C$, represented by the blue curves shown in Figure 4d, in which A is the initial thickness of the whole flake, i.e., ~12 nm, C is the thickness of a single GeAs layer (0.6 nm),[38] and B is a fitting parameter used to simulate a smooth transition in the 70−150 K range.

The model is further corroborated by the estimation of the Debye screening length $L_D = \sqrt{\frac{\epsilon\epsilon_0 kT}{q^2\varphi}}$, which gives the length over which the electric field strength drops by a factor $1/e$ (here $\epsilon = 8$ is the dielectric constant at room temperature of the material[39]). From our data, we estimate $L_D \sim 0.4$ nm at room temperature, confirming that the gate electric field is substantially screened in the layer closer to the gate.

Consistent with our model, we remark that the formation of a conductive channel near the bottom substrate, screening the gate field, and the presence of an energy barrier caused by the inhomogeneous carrier distribution along the channel thickness have been considered to explain the negative transconductance in thick TMD-based back-gated field-effect transistors.[30] Furthermore, the appearance of two separate 2D conductive channels, close to the respective gates, due to S-vacancy ionization and gate-field screening, has been recently reported in dual-gated thick MoS_2 transistors at room temperature. According to such a study, when the temperature is lowered below 80 K, the two separate conductive channels merge into a single one and the top conductive channel governs the transistor behavior.[38]

We also investigated the resistivity behavior ρ as a function of T. The best fitting of the experimental data at low temperature is obtained using the variable-range hopping (VRH) conduction. We notice that VRH is usually observed in amorphous solids as well as in defective systems at low temperature and has been reported in several two-dimensional materials.[40,41] According to VRH theory, the relation between ρ and T can be expressed as[42]

$$\rho(T) = \rho_0 \exp\left(\frac{T_0}{T}\right)^{1/n+1} \tag{5}$$

where ρ_0 depends on the square root of T, T_0 is a constant, and n indicates the dimensionality of the system.[43] Figure 5a shows $\ln(\rho T^{-1/2})$ as a function of $T^{-1/4}$ in the range 20−80 K. The linearity demonstrates that the conduction is bulk type for $T <$

80 K, i.e., it occurs through the entire flake constituting ~20 atomic layers, as assumed in the proposed model. For $T > 180$ K, ρ shows an exponential increase with the inverse of temperature (Figure 5b). This indicates that the thermal excitation of carriers (holes) to the valence band leads to a band-conduction regime, $\rho \propto \exp\left(\frac{E_A}{kT}\right)$, as expected after the formation of a highly conductive 2D channel in the GeAs transistor.

CONCLUSIONS

We fabricated back-gate field-effect transistors with ultrathin GeAs films and investigated their electrical properties over a wide temperature range from 20 to 280 K. We found p-type behavior with temperature upon increasing conductivity. We observed that the carrier density in GeAs flakes depends on temperature with a pronounced and broad peak at around 75 K. We proposed a model based on temperature-dependent channel thickness to explain such an anomaly. We showed that the electrical conduction of the GeAs channel can be explained by variable-range hopping at lower temperatures but it becomes the band-type at higher temperatures when a highly conducting 2D channel is formed. The proposed model, validated by numerical simulation, shows an excellent agreement with the experimental data.

This study provides a new understanding of the intrinsic properties of few-layer GeAs as the channel of field-effect transistors, providing evidence of the formation of a 2D channel limited to a single atomic layer and could be applied to other ultrathin layered materials.

AUTHOR INFORMATION

Corresponding Authors

Antonio Di Bartolomeo − *Physics Department "E. R. Caianiello", University of Salerno, Fisciano 84084, Italy; CNR-SPIN Salerno, Fisciano 84084, Italy;* orcid.org/0000-0002-3629-726X; Email: adibartolomeo@unisa.it

Luca Camilli − *Department of Physics, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark;* orcid.org/0000-0003-2498-0210; Email: lcam@dtu.dk

Authors

Alessandro Grillo − *Physics Department "E. R. Caianiello", University of Salerno, Fisciano 84084, Italy; CNR-SPIN Salerno, Fisciano 84084, Italy;* orcid.org/0000-0002-8909-9865

Francesca Urban − *Physics Department "E. R. Caianiello", University of Salerno, Fisciano 84084, Italy; CNR-SPIN Salerno, Fisciano 84084, Italy;* ⊙ orcid.org/0000-0003-2109-1370

Maurizio Passacantando − *Department of Physical and Chemical Science, University of L'Aquila and CNR-SPIN L'Aquila, L'Aquila 67100, Coppito, Italy;* ⊙ orcid.org/0000-0002-3680-5295

Jose M. Caridad − *Department of Physics, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark*

Jianbo Sun − *Department of Physics, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark;* ⊙ orcid.org/0000-0001-9741-8726

Complete contact information is available at:
https://pubs.acs.org/10.1021/acsami.0c00348

Notes
The authors declare no competing financial interest.

■ REFERENCES

(1) Novoselov, K. S.; et al. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666−669.

(2) Fiori, G.; Bonaccorso, F.; Iannaccone, G.; Palacios, T.; Neumaier, D.; Seabaugh, A.; Banerjee, S. K.; Colombo, L. Electronics Based on Two-Dimensional Materials. *Nat. Nanotechnol.* **2014**, *9*, 768−779.

(3) Lemme, M. C.; Li, L.-J.; Palacios, T.; Schwierz, F. Two-Dimensional Materials for Electronic Applications. *MRS Bull.* **2014**, *39*, 711−718.

(4) Manzeli, S.; Ovchinnikov, D.; Pasquier, D.; Yazyev, O. V.; Kis, A. 2D Transition Metal Dichalcogenides. *Nat. Rev. Mater.* **2017**, *2*, No. 17033.

(5) Jiao, Y.; Hafez, A. M.; Cao, D.; Mukhopadhyay, A.; Ma, Y.; Zhu, H. Metallic MoS_2 for High Performance Energy Storage and Energy Conversion. *Small* **2018**, *14*, No. 1800640.

(6) Di Bartolomeo, A.; Urban, F.; Passacantando, M.; McEvoy, N.; Peters, L.; Iemmo, L.; Luongo, G.; Romeo, F.; Giubileo, F. A WSe2 Vertical Field Emission Transistor. *Nanoscale* **2019**, *11*, 1538−1548.

(7) Urban, F.; Martucciello, N.; Peters, L.; McEvoy, N.; Di Bartolomeo, A. Environmental Effects on the Electrical Characteristics of Back-Gated WSe2 Field-Effect Transistors. *Nanomaterials* **2018**, *8*, 901.

(8) Seo, J.-W. T.; Zhu, J.; Sangwan, V. K.; Secor, E. B.; Wallace, S. G.; Hersam, M. C. Fully Inkjet-Printed, Mechanically Flexible MoS_2 Nanosheet Photodetectors. *ACS Appl. Mater. Interfaces* **2019**, *11*, 5675−5681.

(9) Di Bartolomeo, A.; Genovese, L.; Foller, T.; Giubileo, F.; Luongo, G.; Croin, L.; Liang, S.-J.; Ang, L. K.; Schleberger, M. Electrical Transport and Persistent Photoconductivity in Monolayer MoS_2 Phototransistors. *Nanotechnology* **2017**, *28*, No. 214002.

(10) Patel, A. B.; Machhi, H. K.; Chauhan, P.; Narayan, S.; Dixit, V.; Soni, S. S.; Jha, P. K.; Solanki, G. K.; Patel, K. D.; Pathak, V. M. Electrophoretically Deposited $MoSe_2$/WSe_2 Heterojunction from Ultrasonically Exfoliated Nanocrystals for Enhanced Electrochemical Photoresponse. *ACS Appl. Mater. Interfaces* **2019**, *11*, 4093−4102.

(11) Grillo, A.; Giubileo, F.; Iemmo, L.; Luongo, G.; Urban, F.; Di Bartolomeo, A. Space Charge Limited Current and Photoconductive Effect in Few-Layer MoS_2. *J. Phys.: Conf. Ser.* **2019**, *1226*, No. 012013.

(12) Liu, H.; Cui, M.; Dang, C.; Wen, W.; Wang, X.; Xie, L. Two-Dimensional WSe2/Organic Acceptor Hybrid Nonvolatile Memory Devices Based on Interface Charge Trapping. *ACS Appl. Mater. Interfaces* **2019**, *11*, 34424−34429.

(13) Iemmo, L.; Urban, F.; Giubileo, F.; Passacantando, M.; Di Bartolomeo, A. Nanotip Contacts for Electric Transport and Field Emission Characterization of Ultrathin MoS2 Flakes. *Nanomaterials* **2020**, *10*, No. 106.

(14) Wu, P.; Huang, M. Stability, Bonding, and Electronic Properties of Silicon and Germanium Arsenides: Stability, Bonding, and Electronic Properties of Si and Ge Arsenides. *Phys. Status Solidi B* **2016**, *253*, 862−867.

(15) Jung, C. S.; Kim, D.; Cha, S.; Myung, Y.; Shojaei, F.; Abbas, H. G.; Lee, J. A.; Cha, E. H.; Park, J.; Kang, H. S. Two-Dimensional GeAs with a Visible Range Band Gap. *J. Mater. Chem. A* **2018**, *6*, 9089−9098.

(16) Cheng, A.-Q.; He, Z.; Zhao, J.; Zeng, H.; Chen, R.-S. Monolayered Silicon and Germanium Monopnictide Semiconductors: Excellent Stability, High Absorbance, and Strain Engineering of Electronic Properties. *ACS Appl. Mater. Interfaces* **2018**, *10*, 5133−5139.

(17) Shojaei, F.; Kang, H. S. Electronic Structures and Li-Diffusion Properties of Group IV−V Layered Materials: Hexagonal Germanium Phosphide and Germanium Arsenide. *J. Phys. Chem. C* **2016**, *120*, 23842−23850.

(18) Miao, M.-s.; Botana, J.; Zurek, E.; Hu, T.; Liu, J.; Yang, W. Electron Counting and a Large Family of Two-Dimensional Semiconductors. *Chem. Mater.* **2016**, *28*, 1994−1999.

(19) Lee, K.; Kamali, S.; Ericsson, T.; Bellard, M.; Kovnir, K. GeAs: Highly Anisotropic van Der Waals Thermoelectric Material. *Chem. Mater.* **2016**, *28*, 2776−2785.

(20) Rau, J. W.; Kannewurf, C. R. Optical Absorption, Reflectivity, and Electrical Conductivity in GeAs and GeAs2. *Phys. Rev. B* **1971**, *3*, 2581−2587.

(21) Guo, J.; Liu, Y.; Ma, Y.; Zhu, E.; Lee, S.; Lu, Z.; Zhao, Z.; Xu, C.; Lee, S.-J.; Wu, H.; Kovnir, K.; Huang, Y.; Duan, X. Few-Layer GeAs Field-Effect Transistors and Infrared Photodetectors. *Adv. Mater.* **2018**, *30*, No. 1705934.

(22) Yang, S.; Yang, Y.; Wu, M.; Hu, C.; Shen, W.; Gong, Y.; Huang, L.; Jiang, C.; Zhang, Y.; Ajayan, P. M. Highly In-Plane Optical and Electrical Anisotropy of 2D Germanium Arsenide. *Adv. Funct. Mater.* **2018**, *28*, No. 1707379.

(23) Blachnik, R.; Irle, E. Das System Gallium-Tellur. *J. Less-Common Met.* **1985**, *113*, L1−L3.

(24) Zhou, L.; Guo, Y.; Zhao, J. GeAs and SiAs Monolayers: Novel 2D Semiconductors with Suitable Band Structures. *Phys. E* **2018**, *95*, 149−153.

(25) Mortazavi, B.; Shahrokhi, M.; Cuniberti, G.; Zhuang, X. Two-Dimensional SiP, SiAs, GeP and GeAs as Promising Candidates for Photocatalytic Applications. *Coatings* **2019**, *9*, 522.

(26) Huang, S.; Tatsumi, Y.; Ling, X.; Guo, H.; Wang, Z.; Watson, G.; Puretzky, A. A.; Geohegan, D. B.; Kong, J.; Li, J.; Yang, T.; Saito, R.; Dresselhaus, M. S. In-Plane Optical Anisotropy of Layered Gallium Telluride. *ACS Nano* **2016**, *10*, 8964−8972.

(27) Di Bartolomeo, A.; Grillo, A.; Urban, F.; Iemmo, L.; Giubileo, F.; Luongo, G.; Amato, G.; Croin, L.; Sun, L.; Liang, S.-J.; Ang, L. K. Asymmetric Schottky Contacts in Bilayer MoS2 Field Effect Transistors. *Advanced Functional Materials* **2018**, *28*, No. 1800657.

(28) Bartolomeo, A. D.; Giubileo, F.; Romeo, F.; Sabatino, P.; Carapella, G.; Iemmo, L.; Schroeder, T.; Lupina, G. Graphene Field Effect Transistors with Niobium Contacts and Asymmetric Transfer Characteristics. *Nanotechnology* **2015**, *26*, No. 475202.

(29) Di Bartolomeo, A.; Santandrea, S.; Giubileo, F.; Romeo, F.; Petrosino, M.; Citro, R.; Barbara, P.; Lupina, G.; Schroeder, T.; Rubino, A. Effect of Back-Gate on Contact Resistance and on

Channel Conductance in Graphene-Based Field-Effect Transistors. *Diamond Relat. Mater.* **2013**, *38*, 19−23.

(30) Liu, Y.; Guo, J.; He, Q.; Wu, H.; Cheng, H.-C.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X. Vertical Charge Transport and Negative Transconductance in Multilayer Molybdenum Disulfides. *Nano Lett.* **2017**, *17*, 5495−5501.

(31) Di Bartolomeo, A.; Genovese, L.; Giubileo, F.; Iemmo, L.; Luongo, G.; Foller, T.; Schleberger, M. Hysteresis in the Transfer Characteristics of MoS$_2$ Transistors. *2D Mater.* **2017**, *5*, No. 015014.

(32) Liu, N.; Baek, J.; Kim, S. M.; Hong, S.; Hong, Y. K.; Kim, Y. S.; Kim, H.-S.; Kim, S.; Park, J. Improving the Stability of High-Performance Multilayer MoS$_2$ Field-Effect Transistors. *ACS Appl. Mater. Interfaces* **2017**, *9*, 42943−42950.

(33) Urban, F.; Giubileo, F.; Grillo, A.; Iemmo, L.; Luongo, G.; Passacantando, M.; Foller, T.; Madauß, L.; Pollmann, E.; Geller, M. P.; Oing, D.; Schleberger, M.; Di Bartolomeo, A. Gas Dependent Hysteresis in MoS$_2$ Field Effect Transistors. *2D Mater.* **2019**, *6*, No. 045049.

(34) Di Bartolomeo, A.; Pelella, A.; Liu, X.; Miao, F.; Passacantando, M.; Giubileo, F.; Grillo, A.; Iemmo, L.; Urban, F.; Liang, S. Pressure-Tunable Ambipolar Conduction and Hysteresis in Thin Palladium Diselenide Field Effect Transistors. *Adv. Funct. Mater.* **2019**, *29*, No. 1902483.

(35) Han, K. H.; Kim, G.-S.; Park, J.; Kim, S.-G.; Park, J.-H.; Yu, H.-Y. Reduction of Threshold Voltage Hysteresis of MoS$_2$ Transistors with 3-Aminopropyltriethoxysilane Passivation and Its Application for Improved Synaptic Behavior. *ACS Appl. Mater. Interfaces* **2019**, *11*, 20949−20955.

(36) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*, 3rd ed.; Wiley-Interscience: Hoboken, NJ, 2007.

(37) Ang, Y. S.; Yang, H. Y.; Ang, L. K. Universal Scaling Laws in Schottky Heterostructures Based on Two-Dimensional Materials. *Phys. Rev. Lett.* **2018**, *121*, No. 056802.

(38) Ji, H.; Ghimire, M. K.; Lee, G.; Yi, H.; Sakong, W.; Gul, H. Z.; Yun, Y.; Jiang, J.; Kim, J.; Joo, M.-K.; Suh, D.; Lim, S. C. Temperature-Dependent Opacity of the Gate Field Inside MoS$_2$ Field-Effect Transistors. *ACS Appl. Mater. Interfaces* **2019**, *11*, 29022−29028.

(39) Mead, D. G. Long Wavelength Study of Semiconducting Germanium Arsenide, GeAs. *Infrared Phys.* **1982**, *22*, 209−213.

(40) Ghatak, S.; Pal, A. N.; Ghosh, A. Nature of Electronic States in Atomically Thin MoS$_2$ Field-Effect Transistors. *ACS Nano* **2011**, *5*, 7707−7712.

(41) Choi, S. J.; Kim, B.-K.; Lee, T.-H.; Kim, Y. H.; Li, Z.; Pop, E.; Kim, J.-J.; Song, J. H.; Bae, M.-H. Electrical and Thermoelectric Transport by Variable Range Hopping in Thin Black Phosphorus Devices. *Nano Lett.* **2016**, *16*, 3969−3975.

(42) Mott, N. F. Conduction in Glasses Containing Transition Metal Ions. *J. Non-Cryst. Solids* **1968**, *1*, 1−17.

(43) Barreteau, C.; Michon, B.; Besnard, C.; Giannini, E. High-Pressure Melt Growth and Transport Properties of SiP, SiAs, GeP, and GeAs 2D Layered Semiconductors. *J. Cryst. Growth* **2016**, *443*, 75−80.