Thermal characterization of the $SiO_2 - Ge_2Sb_2Te_5$ interface from room temperature up to $400\,°C$ ⊘

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Thermal characterization of the SiO$_2$-Ge$_2$Sb$_2$Te$_5$ interface from room temperature up to 400 °C

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The thermal conductivity of Ge$_2$Sb$_2$Te$_5$ (GST) layers, as well as the thermal boundary resistance at the interface between the GST and amorphous SiO$_2$, was measured using a photothermal radiometry experiment. The two phase changes in the Ge$_2$Sb$_2$Te$_5$ were retrieved, starting from the amorphous and sweeping to the face centered cubic (fcc) crystalline state at 130 °C and then to the hexagonal crystalline phase (hcp) at 310 °C. The thermal conductivity resulted to be constant in the amorphous phase, whereas it evolved between the two crystalline states. The thermal boundary resistance at the GST-SiO$_2$ interface was estimated to be higher for the hcp phase than for the amorphous and fcc ones. © *2010 American Institute of Physics*. [doi:10.1063/1.3284084]

I. INTRODUCTION

Phase change materials are extensively studied due to their promising applications in the framework of phase change memory (PCM) or ovonic unified memory.[1,2] PCM functioning involves chalcogenide materials that are allotropic semiconducting elements and alloys belonging to the IV, V, and VI group of the periodic classification. They can be reversibly brought from the amorphous to the crystalline state so that the corresponding different electrical properties can be used for data storage. Ge$_2$Sb$_2$Te$_5$, commonly denoted as GST, is one of the most popular chalcogenides[3] since it is stable at room temperature (RT) in the amorphous and hexagonal close packed (hcp) phase and metastable in the face centered cubic phase (fcc).[4,5] The transition temperature is ~130 °C for the fcc-crystalline phase and ~350 °C for hcp-crystalline phase, whereas the melting temperature is approximately 600 °C. The transformation between crystalline and amorphous phases is reversible: heating the amorphous GST to a temperature slightly above the glass-transition temperature leads to the crystalline phase; subsequent heating to a temperature close to the melting temperature with fast quenching permits retrieving the amorphous phase. A change in the density of the material is observed for each state[6] (~6.4 g cm^{-3} in the hcp-crystalline state, ~6.3 g cm^{-3} in the fcc-crystalline state, and ~5.9 g cm^{-3} in the amorphous state). The specific heat of the GST is not dependent on its crystallographic phase and can be considered equal to $C_{p\text{-GST}}=212$ J kg^{-1} K^{-1} (within the 20–400 °C temperature range).

Each phase is characterized by different optical[7] and electrical[2] properties that also depend on the deposition parameters.[8] The electrical resistivity varies over several decades, according to the phase: in the amorphous state GST is an insulator (up to 1 Ω m), whereas in the crystalline state, it becomes conductive (10^{-4}–10^{-3} Ω m for the fcc crystalline and about 10^{-5} Ω m for the hcp crystalline).[9] Previous work[10] has shown that the thermal conductivity of GST does not exhibit such a large variation during the phase change transformation. Nevertheless, even if the variation remains small, the thermal conductivity is a sensitive parameter when simulating the heat transfer in a memory device based on such a phase change material. Some authors[10,11] reported $k_{\text{GST}} \approx 0.2$ W m^{-1} K^{-1} as the experimental thermal conductivity value of the GST in its amorphous phase, $k_{\text{GST}} \approx 0.5$ W m^{-1} K^{-1} in its fcc-crystalline phase, and $k_{\text{GST}} \approx 1.4$ W m^{-1} K^{-1} in the hcp-crystalline phase. The value for the fcc-crystalline state seems also to be in good agreement with that predicted by the Debye's model. On the other hand, the model of Cahill[12] gives a value of the minimum thermal conductivity of GST in its amorphous state that is in reasonable agreement with the measured one (however, this model requires also knowing the sound velocity inside the medium).

Kencke *et al.*[13] measured the electrical resistance, as well as the thermal boundary resistance (TBR) at the interface between the bottom electrode (BE) and amorphous GST, for a phase change memory cell. The experimental procedure was based on the nanosecond thermoreflectance technique in the 25–100 °C temperature range and a TBR value for the BE-GST layers was obtained approximately equal to $R_i=3.5\times10^{-8}$ K m^2 W^{-1}. Reifenberg *et al.*[14] demonstrated the influence of the BE-GST TBR on the programming current: the programming current decreases as the TBR increases. Therefore, they proposed different technological solutions to increase the TBR, such as the deliberate introduction of interface disorder or the insertion of low conductive thin films between the BE and the GST layer (Kim *et al.*[15] proposed inserting a 30 nm thick fullerene film). The motivation in seeking the TBR between each layer that constitutes the memory cell is based on the usefulness of a very simple calculus. Indeed, the thermal resistance of a 40 nm

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FIG. 1. SEM cross-sectional image obtained after the sample had been thermally characterized. After the 400 °C annealing temperature is reached, the GST crystalline phase is observed. It is also seen that the Pt layer thickness remains unchanged during the characterization.

thick GST layer in the hcp phase is $40 \times 10^{-9}/1.4 = 2.9 \times 10^{-8}$ K m² W⁻¹, which is very close to the measured TBR between the GST and the BE. In such a case, the TBR must be introduced as a fundamental parameter for multiphysics (electrical and heat transfer) simulation of the PCM. Unfortunately, it is very difficult to theoretically estimate the TBR value at high temperatures. Most of the theoretical models on the TBR between two solid media, neglecting the influence of roughness, are based on acoustic mismatch and diffuse mismatch that do not fit with the experiments when the temperature is high with respect to the Debye temperature.[16,17] An interesting approach to model the heat transfer at the interface between two solid layers at high temperature is to perform a nonequilibrium molecular dynamics simulation.[18]

The TBR at the interface between the GST and the dielectric material (usually silicon oxide or silicon nitride) used in the memory cell can also have a significant influence on the heat transfer balance and thus on the electrothermal response.

In this paper, we investigated the thermal conductivity of the GST layer, as well as the TBR at the interface between GST and amorphous SiO₂, depending on temperature, from RT up to 400 °C. Starting from the amorphous state, the GST was swept to the fcc- and hcp-crystalline states by increasing the temperature.

II. EXPERIMENTAL PROCEDURE AND MATHEMATICAL GOVERNING EQUATIONS

The reference amorphous SiO₂ (α-SiO₂) layer was obtained using a rapid thermal annealing of a Si wafer, yielding a 100 nm thick amorphous SiO₂ layer, whose thermal conductivity was measured through the photothermal radiometry (PTR) technique to be equal to $k_{SiO_2} = 1.45$ W m⁻¹ K⁻¹. By increasing the temperature, we found that the thermal conductivity of α-SiO₂ does not vary significantly up to 400 °C.

In order to discriminate the GST thermal conductivity from the TBR (R_i) at the GST-SiO₂ interface, five samples with different GST thicknesses, namely, 100, 210, 420, 630, and 840 nm, were prepared, The deposition of GST was achieved using dc-magnetron sputtering on a 100 nm thick thermally grown α-SiO₂ on Si substrate. Each thickness was carefully measured by field-emission scanning electron microscopy (SEM). An illustration for the 210 nm GST is given in Fig. 1; this SEM image was obtained after the thermal characterization of the sample, which means that the GST

had been annealed and therefore it is in the crystalline state (crystalline grains can be distinguished in the image). However, it must be emphasized that the maximum thickness that can be deposited during the sputtering process is 210 nm. This means that 420, 630, and 840 nm GST thick layers are achieved in 2, 3, and 4 deposition steps, respectively. Therefore, different interfaces are present inside the GST layers (1 for 420 nm, 2 for 630 nm, and 3 for 840 nm); these interfaces can have significant influence on heat transfer during the characterization.

Assuming that the Fourier law is valid in both the SiO₂ and GST layers, the thermal resistance of the GST-SiO₂ stack is defined as

$$R = \underbrace{R_{GST} + R_i}_{R_t} + R_{SiO_2} = \frac{e_{GST}}{k_{GST}} + R_i + \frac{e_{SiO_2}}{k_{SiO_2}}. \quad (1)$$

In this relation, R_i denotes the TBR at the GST-SiO₂ interface, R_{SiO_2} denotes the thermal resistance of the SiO₂ layer, and R_{GST} is the thermal resistance of the GST layer. In this relation, e_{SiO_2} and e_{GST} are the thicknesses of the GST and SiO₂ layers, respectively.

Using ellipsometry we found that the extinction coefficient for GST at 514 nm (the wavelength of the laser used in the PTR) varies between 2.5 and 4.5 in the amorphous and crystalline fcc states, respectively. With respect to the GST layer thicknesses, this coefficient leads to a non-negligible optical depth absorption (~ 17 nm) at 514 nm. Therefore, a platinum layer (30 nm thick) was deposited by e-beam evaporation on the GST layer as a transducer for the incident laser beam. Indeed, the heat flux is absorbed by the Pt layer that is assumed to be isothermal for all the frequency range swept during the experiment; on the other hand, the Pt layer avoids possible oxidation and evaporation of the GST at high temperature. Moreover, it must be also noted that thermoluminescence of the silicon substrate occurs at ~ 1.7 μm. Since the GST is transparent at such a wavelength, this radiation can be collected by the IR detector. Capping the GST with the Pt layer limits this thermoluminescence radiation from the sample surface so that only the radiation related to heat transfer in the sample is measured.

PTR experiments were implemented to measure the thermal resistance R [as defined in relation (1)] of each sample as a function of temperature. The basic principle is to measure the phase lag and the amplitude of the periodic temperature response produced on the sample surface by a modulated laser beam.[19] A thermal diffusion model describing the heat transfer in the sample during the experiment enables the calculation of the theoretical phase lag and the amplitude as a function of frequency. The identification of the stack thermal resistance is performed by minimization of the gap between the theoretical and the experimental data.

The schematic view of the PTR experimental setup is presented in Fig. 2. In order to perform experiments at different temperatures, the temperature of the sample was controlled by a commercially available heating device, working under argon as inert gas. The sample was heated at a rate of 20 °C/min and annealed for 5 min at the required
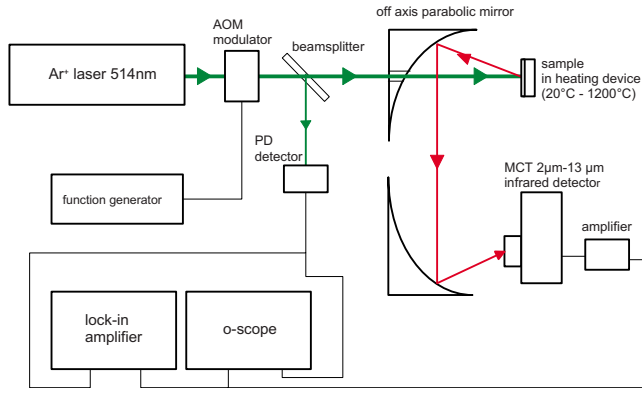
FIG. 2. (Color online) PTR experimental setup. The sample is put inside a furnace that permits reaching 1200 °C under vacuum or under inert gas.
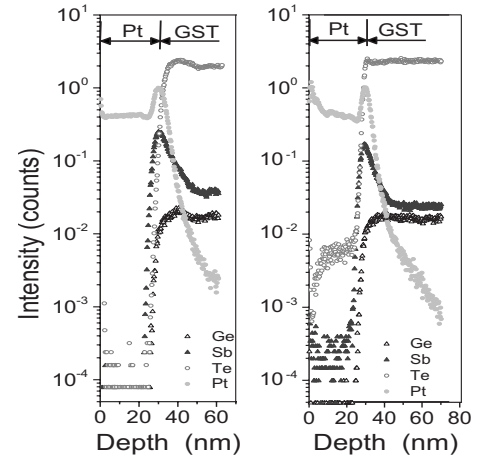

FIG. 3. ToF-SIMS analysis obtained from the 210 nm thick GST sample. It is observed a small diffusion of Pt inside the GST that leads to consider that the TBR at the Pt-GST interface is negligible with respect to that at the GST-SiO$_2$ interface.

temperature before starting the measurement. Optical access to the sample located inside the crucible of the heating device was ensured by a BaF$_2$ window that is transparent in the visible and infrared radiation range. The thermal excitation was generated on the sample front face by an Ar$^+$ laser of 514 nm wavelength and 1.7 W maximum power. The laser was modulated by an acousto-optic modulator using the square signal issued from a function generator and was reflected to the sample surface by a set of mirrors. The laser beam had a Gaussian profile of power repartition on the spot of 1 mm in diameter at $1/e^2$. A very fast photodiode was used to measure the reference signal, in order to avoid the phase lag due to the acousto-optic modulator driver. The thermal response was measured by an infrared HgCdTe detector. The wavelength measurement range of this IR detector was comprised between 2 and 13 μm. Parabolic mirrors coated with high reflective rhodium (reflectivity of 98% in the infrared detector wavelength band) were used to collect the emitted infrared radiation and to focus it on the infrared detector. The detector wavelength operating range was higher than that of the laser, therefore, the measurement was not disturbed by the photonic source; moreover, an optical filter was used in order to reject all the visible radiation arriving on the IR detector. The zone viewed by the detector was the image of the infrared sensitive element on the sample corresponding to a circle of 1 mm in diameter. A lock-in amplifier was used to measure the amplitude and the phase lag between the reference and the detector output, according to the frequency. The frequency range of 1–100 kHz, where the phase and the amplitude are sensitive to the thermal resistance of the film, was swept during the experiment. Each measurement for the amplitude and phase was affected by a 5% standard deviation. The periodic temperature variation ΔT at the sample surface was small enough to assume that the measured radiative emission by the IR detector was linearly proportional to ΔT.

Considering the large diameter of the laser beam with respect to the small GST film thicknesses, the heat transfer in the sample in this experimental configuration is described by the following relations in one dimension

$$\frac{1}{\alpha_i}\frac{\partial T}{\partial t} = \frac{\partial^2 T}{\partial z^2}, \quad 0 \leqslant z \leqslant e_i, \quad t > 0, \quad i = \text{GST}, \text{SiO}_2, \text{Si}.$$

$$(2)$$

With related boundary conditions

$$-k_{\text{GST}}\frac{\partial T}{\partial z} = \varphi_0 \cos(\omega t), \quad z = 0, \quad t > 0, \tag{3}$$

$$T = 0, \quad z = e_T = e_{\text{GST}} + e_{\text{SiO}_2} + e_{\text{Si}}, \quad t > 0, \tag{4}$$

$$T_{\text{GST}} - T_{\text{SiO}_2} = R_i\varphi, \quad z = e_{\text{GST}}, \quad t > 0, \tag{5}$$

and the initial condition

$$T = 0, \quad 0 \leqslant z \leqslant e_T, \quad t = 0, \tag{6}$$

where α_i is the thermal diffusivity $(k_i/\rho_i C_i)$ of the respective layer i, T is the temperature, t is the time, and φ is the heat flux. Condition (3) corresponds to the periodic heat flux with angular frequency $\omega = 2\pi f$. Equation (4) gives the condition of prescribed temperature (after a change in variable) and initial condition.(6) The boundary condition (5) introduces the thermal resistance at the GST-SiO$_2$ interface. We performed a time of flight secondary ion mass spectroscopy (ToF-SIMS) experiment using an ION-TOF IV instrument, on the 210 nm thick GST sample. ToF-SIMS measurements were taken sputtering over 200×200 μm^2 area Cs$^+$ ions with energy of $E = 500$ eV and analyzing a 50×50 μm^2 at the center of the sputtered area with Ga$^+$ ions with energy of $E = 25$ keV, and collecting secondary (sputtered) negative ions. The result is presented in Fig. 3 and shows a small diffusion of the Pt inside the GST at the interface. This located mixing at the Pt-GST interface leads us to assume a negligible thermal resistance at the Pt-GST interface with respect to the GST-SiO$_2$ interface. Furthermore, SIMS measurement on the annealed sample at 400 °C does not show a change in the Pt layer as well as at the GST-Pt interface, which denotes that the Pt does not diffuse more inside the GST layer when increasing the temperature. Thus, previous assumption remains valid for all the swept temperature
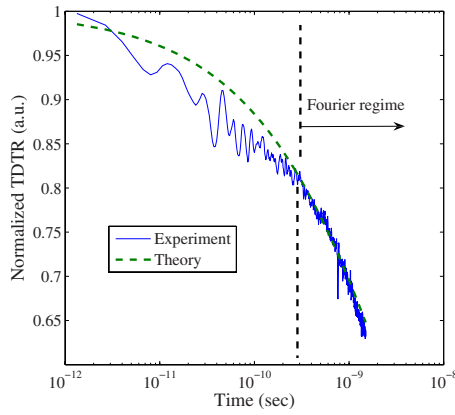
FIG. 4. (Color online) Plot of a TDTR experiment performed on a hcp-GST layer, 420 nm thick, capped with a 55 nm aluminum film. The simulation exhibits the time range needed for the Fourier regime to become applicable.

ranges. On the other hand, the SiO_2-Si interface does not act in this configuration since the amorphous oxide is achieved by thermal annealing.

The system of partial differential equations was solved using the Laplace integral transform on time.[19] The unknown thermal resistance $R_t = R_i + R_{GST}$ is identified using a minimization procedure based on the large-scale algorithm. This algorithm is a subspace trust region method and is based on the interior-reflective Newton method described in Ref. 20. It must be noticed that each iteration involves the approximate solution of a large linear system using the method of preconditioned conjugate gradients. The thermal conductivity of GST and the TBR are retrieved using the thermal resistances identified for each thickness of the GST film.

A. Validation of the Fourier regime assumption

The goal of this section is to justify the use of relation (1), i.e., the expression of the thermal resistance of each layer (GST and α-SiO_2) according to their respective thicknesses and thermal conductivities ($R = e/k$). We first performed a picosecond time domain thermoreflectance (TDTR) experiment on the 400 nm thick GST layer in the hcp-crystalline phase at RT. The experimental method is described in the paper of Battaglia *et al.*[21] and was based on a time resolved pump-probe setup using ultrashort laser pulses (wavelength =800 nm and pulse duration $\tau = 100$ fs) generated by a Ti:sapphire laser. The transducer was an aluminum film [denoted as Al, with $e_{Al} = 55$ nm for the thickness and $\rho C_p(Al) = 2700 \times 900$ J kg^{-1} m^{-3} of specific heat per volume unit], deposited on the GST layer in order to increase the signal-noise ratio during the TDTR. The expression of the average (with respect to the spatial distribution of the temperature on the heated area) normalized time domain thermoreflectance signal is $\widetilde{TDTR} = \exp(\alpha^2 t) \mathrm{erfc}(\alpha \sqrt{t})$, where $\alpha = E_{GST}\widetilde{\beta_h}/C_p(Al)$, $E_{GST} = \sqrt{k_{GST}\rho C_p(GST)}$ is the effusivity of the GST layer, and $1/\widetilde{\beta_h} = e_{Al}$ is the heat penetration depth during the thermallization process between electrons and the lattice in the aluminum film. The result of the experiment is reported in Fig. 4, as well as the simulation obtained from the heat conduction model. It clearly appears that the measured impulse response fits very well with the semi-infinite
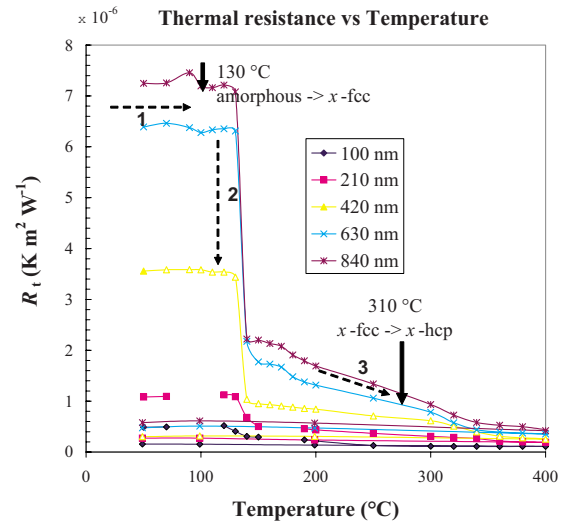

FIG. 5. (Color online) Plot of the measured thermal resistance $R_t = R_{GST} + R_i$ as a function of the temperature of the sample.

behavior when time becomes higher than $\Delta \tau_{min} = 0.3$ ns. This demonstrates that the Fourier law is valid only for GST layers whose thickness is higher than $\min(e_{GST}) \approx \sqrt{\Delta \tau_{min} k_{hcp\text{-}GST}/\rho C_p(GST)} = 19.3$ nm [for this calculus we used $k_{hcp\text{-}GST} = 1.7$ W m^{-1} K^{-1} and $\rho C_p(hcp\text{-}GST) = 6400 \times 212$ J m^{-3} K^{-1}]. This minimal GST thickness is largely inferior to the thicknesses of the used GST samples. This value can be viewed as the phonons mean free path in the hcp-GST and it must be lower in the amorphous phase. Implicitly, it demonstrates also the validity of the framework of the thermophysical properties of GST in the hcp phase. The same experiment was performed on a α-SiO_2 layer and it was found that $\min(e_{\alpha\text{-}SiO_2}) \approx 5.3$ nm.

III. RESULTS AND ANALYSIS

Figure 5 represents the measured thermal resistance R_t according to the temperature for all the Pt/GST/SiO_2/Si stacks. The thermal resistance before the α-fcc transition is constant (zone 1) until the phase change occurs at 130 °C (zone 2). The fcc-hcp transition occurs close to 310 °C, but it is not as clearly observable as for the first one since the thermal resistance increases continuously between the two phase change temperatures (zone 3). After reaching 400 °C, the temperature is decreased and it is observed that the thermal resistance remains constant for all the samples, as expected, since the hcp configuration is stable. Figure 6 shows the measured value of R_t as a function of the thickness of the GST layer for the whole swept temperature range. For the α-GST ($T < 100$ °C), the linear regression can be considered only for the first two thicknesses (100, 210 nm). Indeed, it is clear that the thermal resistance increases rapidly for the three higher thicknesses (420, 630, and 840 nm). As said in Sec. I, this phenomenon comes from the fact that these thicknesses are obtained after several deposition steps, each step corresponding to a 210 nm deposition. Therefore, there are the 1, 2 and 3 additional interfaces between each layer inside the GST that lead to a significant increase in the $R_{\alpha\text{-}GST}$ value. On the other hand, results obtained at 140 °C show
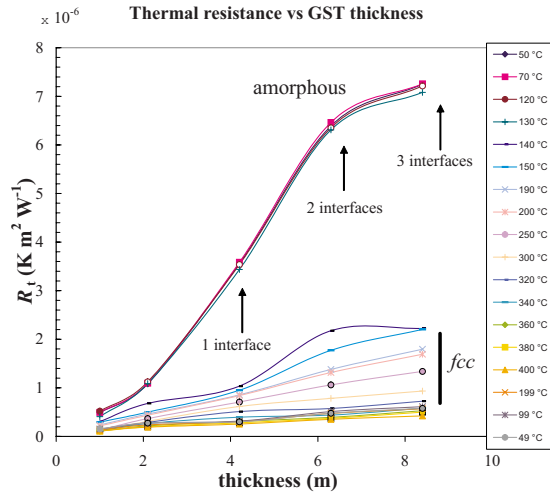
FIG. 6. (Color online) Plot of the measured thermal resistance at different temperatures as a function of the thickness of the GST layer.

FIG. 8. (Color online) Plot of the TBR at the GST-SiO$_2$ interface as a function of temperature. Dots represent the corresponding regression coefficients.

that these interfaces disappear when the GST crystallizes. This means that the intrinsic thermal conductivity for the amorphous phase, as well as the TBR at the α-GST-SiO$_2$ interface, must be calculated from the linear regression obtained for the 100 and 210 nm thick GST only. For the crystalline samples, a linear regression between the thermal resistance and the GST thickness is well retrieved, as expected from relation (1).

Using relation (1) for all the measured values of R_t, the corresponding values of the intrinsic GST thermal conductivity versus temperature were found, as represented in Fig. 7, as well as the variation in the TBR versus temperature, as represented in Fig. 8. Since the precision on the TBR values is strongly dependent on the slope of the curve, the regression coefficients R^2 are also reported in Fig. 8.

Only the values with $0.98 < R^2 < 1$ were retained for the TBR. A constant value of $k_{\alpha\text{-GST}} = 0.19$ W m^{-1} K^{-1} was found for the amorphous phase with a TBR of $R_i = 5 \times 10^{-8}$ K m^2 W^{-1}. The intrinsic thermal conductivity for the fcc-GST varied from $k_{\text{fcc-GST}} = 0.42$ W m^{-1} K^{-1}
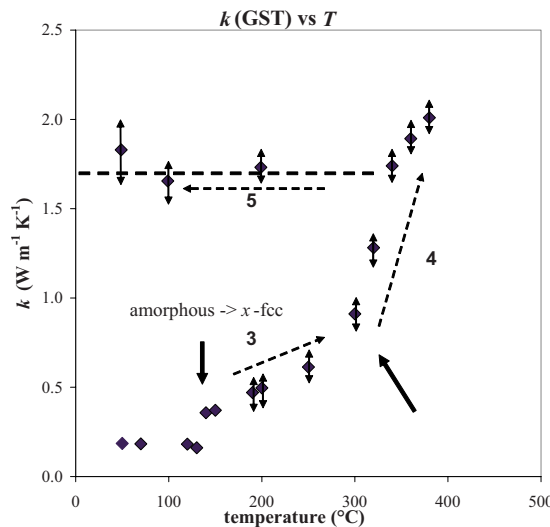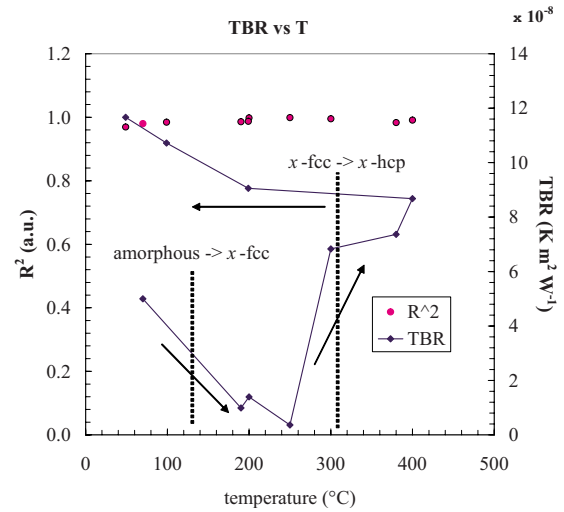
to 0.91 W m^{-1} K^{-1} in the 140–300 °C range. From the phase change temperature to 250 °C, the TBR decreased significantly to reach a minimum value of $R_i = 5 \times 10^{-9}$ K m^2 W^{-1}. Above 250 °C, the TBR increased to 9 $\times 10^{-8}$ K m^2 W^{-1} at 400 °C. The intrinsic thermal conductivity for hcp-GST (from 310 to 400 °C) varied from $k_{\text{hcp-GST}} = 1.1$ to 2 W m^{-1} K^{-1}. Obviously, this particular behavior cannot be observed when one characterizes an annealed sample at RT. Indeed, as it can be seen in Fig. 7, the thermal conductivity of the hcp-phase remained quite constant and equal to 1.6 W m^{-1} K^{-1}. On the other hand, it was found that the TBR between the GST and α-SiO$_2$ is higher ($R_i \approx 1 \times 10^{-7}$ K m^2 W^{-1}, in Fig. 8) for hcp-GST than that for fcc-GST and α-GST.

IV. CONCLUSION

The TBR at the interface between GST and SiO$_2$ thin films is a fundamental parameter that influences the heat transfer in a PCM device. This parameter appears even more dominant as the GST thickness decreases down to the tens of nanometer range. As we demonstrated using the TDTR technique, the Fourier regime for the crystalline hcp-GST phase is applicable when the thickness is higher than 20 nm. An interesting achievement of the present work is that the GST thermal conductivity in the hcp-phase still increases with the temperature. On the other hand, the same literature value was found when the temperature is set back to RT.

According to our results, the thermal resistance of a 40 nm thick GST in the hcp phase is $R_{\text{GST}} = 40 \times 10^{-9}/1.6 = 2.5 \times 10^{-8}$ K m^2 W^{-1} at RT. Since TBR results above 10^{-8} K m^2 W^{-1}, this means that TBR plays a significant role on controlling the heat transfer and should be included in PCM modeling.

ACKNOWLEDGMENTS

FIG. 7. (Color online) Plot of the intrinsic thermal conductivity of the GST as a function of temperature.

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