Development of a Space-Grade Ka-Band MMIC Power Amplifier in GaN/Si Technology for SAR Applications

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***Abstract*— This article presents the complete characterization of a Ka-band monolithic (MMIC) high-power amplifier (HPA) developed with a commercial 100-nm gallium nitride (GaN)/Si process provided by OMMIC (now MACOM). The amplifier was conceived for a space-compliant environment, focusing, in particular, on pulsed radar applications, e.g., for synthetic aperture radar (SAR) altimetry. The amplifier is designed accounting for the critical reliability constraints posed by the space environment. Due to the poorer thermal characteristics of GaN/Si technologies compared with their GaN/SiC counterparts, proper thermal-aware criteria are needed to be exploited during the design process. The fabricated MMIC has been characterized under different biasing and temperature conditions and finally tested with a representative SAR signal. The amplifier achieves at 36 GHz an output power of 10, 8.4, and 6.6 W when biased with a drain voltage of 11.25, 10, and 9 V, respectively, with an associated PAE around 20% and a linear gain of roughly 20 dB under all biasing conditions and with an MMIC backside temperature ranging from −10 °C up to +80 °C. With a 9-V bias, the designed MMIC is fully compliant with the maximum derated junction temperature limit of 160 °C recommended for space reliability in both pulsed and continuous-wave (CW) operations, demonstrating performance well in line with the state of the art for this technology when a space-grade design is required.**

***Index Terms*— Gallium nitride (GaN), GaN-Si, high-power amplifier (HPA), Ka-band, satellites, space derating.**

I. Introduction

GALLIUM nitride (GaN) technology represents a breakthrough in the field of high-power/high-frequency electronics, from high-voltage switching applications to RF and microwave power amplifiers, because of its high power density and breakdown voltage, low ON-resistance, and fast switching [1]. Leading semiconductor foundries today offer subquarter-micrometer gate-length GaN HEMT processes, opening the way to millimeter-wave applications. In particular, Ka-band is regarded as the new reference frequency range for both 5G new radio (5GNR) and satcom systems, as well as for radar and remote sensing applications. This is because of the potentially wide bandwidth achievable, allowing for high data rates and high radar resolution [2], [3], [4].

While, up to 31 GHz, both traditional and advanced high-power amplifier (HPA) architectures have been largely demonstrated [5], [6], [7], [8], achieving high performance up to 35 GHz or higher is still challenging and less reported. Among the HPAs presented in the literature, several rely on in-house or research processes, such as, for example, the semidistributed amplifier proposed in [9], the 9-W HPA in [10], and the 15-W HPA in [11]. Focusing on commercial GaN processes only, the number of HPAs available in the literature that are capable of providing more than 35 dBm of output power up to at least 35 GHz is relatively low, as reported in Table I.

The highest frequency achieved with 200-nm gate-length transistors is 36.5 GHz, as reported in [12], where an MMIC implemented with the Northrop Grumman GAN20 GaN/SiC process is presented. Note that the substrate was thinned to 100 μm. The Qorvo QGaN15 [13], [17] and the UMS GH15 [14], [16] 150-nm GaN/SiC processes also proved to be able to cover frequencies above 35 GHz, but with a substrate thinned to 70 μm or lower. The D01GH and D006GH GaN/Si processes [15], [18], [19], developed by OMMIC (now acquired by MACOM), have 100- and 60-nm gate-length devices, respectively, and OMMIC offers the possibility of using both sized devices on the same MMIC [19], therefore representing a very interesting option for applications targeting the highest portion of the Ka-band. As can be seen from the HPA comparison reported in Table I, because of the better thermal dissipation of the substrate, GaN/SiC technologies achieve sensibly higher output power densities (larger than 2.5 W/mm) than their GaN/Si counterparts, especially when space-grade thermal constraints are considered [19], [20]. On the other hand, GaN/Si offers a neat advantage in terms of fabrication costs and worldwide availability as well as future potential integration with Si-based digital technology.

The work presented here discusses the potential and limitations for space use of the D01GH GaN/Si technology for developing Ka-band HPAs. The work has been developed in

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TABLE I
Ka-BAND MMIC HPAS IN COMMERCIAL-GRADE GaN PROCESSES WITH $f_{max} \geq 35$ GHz AND $P_{out} \geq 3$ W

Ref.	Manufacturer and Technology	Frequency range GHz	Output power dBm	Gain dB	PAE %	P_{out} density W/mm
[12]	NG 0.2 GaN/SiC	34.5 – 36.5	37.7	25	41	NA
[13]	Qorvo 0.15 GaN/SiC	32 – 38	40.5	25	35	3.5
			37.1	17.5	34	3.2
[14]	UMS 0.15 GaN/SiC	29.5 – 36	39.5	19	20	2.8
[15]	OMMIC 0.1 GaN/Si	34 – 38	36.4	30	29.5	2.7
[16]	UMS 0.15 GaN/SiC	26 – 35	39	23	26.5	2.5
[17]	Qorvo 0.15 GaN/SiC	33 – 37	35	20	14	NA
[18]	OMMIC 0.1 GaN/Si	37 – 40	35	17	27	1.7
[19]	OMMIC 0.1 GaN/Si	32 – 36	35	25	16	1.1*
This Work	**OMMIC 0.1 GaN/Si**	**35 – 36**	**40**	**22**	**20**	**1.6**
			38*	**20***	**19***	**1.0***

*Space-compliant results.

the framework of a European Space Agency (ESA) project for remote earth observation, in particular, for a Ka-band radar altimeter operating in the 35.5–36-GHz range, targeting the highest possible reliable output power (compatible with the fixed MMIC dimensions of 4.5 × 4 mm^2), and efficiency, together with a large-signal (LS) power gain of 20 dB. Despite the challenges posed by space derating, the designed HPA demonstrated in measurement an output power between 38 and 40 dBm, depending on the maximum baseplate temperature, with an associated gain in excess of 20 dB and PAE around 20% in the 35–36-GHz bandwidth. The achieved results are well in line with the state of the art at this frequency, even considering terrestrial applications as reported in Table I, demonstrating the suitability of this technology for space applications. A larger bandwidth has been demonstrated in [19], however relaxing the requirements on output power and efficiency, or in [15] and [18], relaxing also requirements on junction temperature.

This article is organized as follows. In Section II, the design of the MMIC HPA, briefly introduced in [21], is detailed, highlighting circuit topology and design choices adopted to meet recommended space derating rules [22]. In Section III, measurement results are provided and compared with simulations along with a description of the MMIC test jig and measurement setup. Conclusions and discussion of future developments are then provided in Section IV.

II. MMIC DESIGN

The objective of the project was to develop a high-power amplifier (HPA) suitable for space applications, adopting GaN/Si technology at 36-GHz frequency, adhering to a maximum MMIC size of 4.5 × 4 mm^2.

The target application is an altimeter operated in synthetic aperture radar (SAR) closed-burst mode [23]: a form of closed-loop altimeter tracking where the pulses are transmitted and received in bursts rather than interleaved radar operation. In the specific case, the expected duty cycle is very high (roughly 90%), hence very close to continuous-wave (CW) conditions. Therefore, as a worst case for thermal stress, the design has been developed, considering CW operation.

Considering the nominal process performance presented in [24] (3.3-W/mm output power density) for the same technology and with the suggestions from the foundry regarding space derating, an output power in the 8–10-W range was targeted. The feasibility of this target for a space-grade HPA was also confirmed by the simulations reported in [25] and [26]. As in every payload circuit, efficiency maximization is another critical and challenging constraint. In this case, the radar altimeter required only one MMIC HPA, and not several hundreds as in applications involving active antennas [27], thus implying that the efficiency of the amplifier has not a direct effect on the system performance. However, it is still fundamental to maximize the efficiency, since the HPA output power is limited by thermal reliability constraints as detailed in the following description. Finally, a value of about 20 dB was selected as the target LS gain.

A. Space-Compliant (Thermal-Aware) Design

Power amplifier design for space applications requires special cautionary measures, due to both the stressing environmental conditions at which the HPA will operate, which can rapidly degrade its lifetime and reliability, and the necessity to guarantee the mission timespan without failures due to the impossibility of component replacement. To overcome such issues, derating rules are applied to all onboard electronic equipment: in particular, component oversizing and power supply reduction are two derating procedures required by space-grade HPA design. To avoid overderating, standard regulations have also been developed worldwide [22], [28]. Thermal stress is a major concern for HPAs, since MMIC cooling in space environment is particularly difficult. Consequently, the chip must be conceived to work with reduced maximum junction temperature, recommended by ESA to be 160 °C for GaN technology [22]. This condition must be enforced up to the maximum expected backside temperature, which in space can reach the 75 °C–85 °C range, which clearly results in an extremely small maximum allowed dissipated power. A rough quantification of this limitation with respect to a commercial application is helpful: for a base-station product, typical HPA performance is given at room temperature (25 °C) given the possibility to cool the HPA base plate, and the maximum junction temperature is typically 200 °C for commercial-grade reliability. This gives an allowed temperature rise of 175 °C, which is more than twice than the roughly 80 °C temperature rise allowed in space (considering 80 °C base plate and 160 °C maximum junction temperature). Even neglecting the typical thermal resistance increase with temperature, from the previous considerations it comes out that, for the same technology, a space-grade HPA can typically target no more than half of the power density

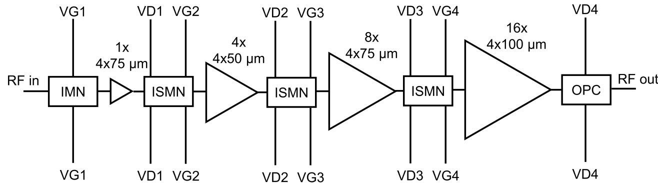


Fig. 1. Structure of the Ka-band MMIC HPA.

of a commercial-grade one [29], [30]. This limitation is more pronounced in GaN/Si technologies, as they are further limited by the poor thermal conductivity of the substrate (silicon in this case), implying, with respect to the GaN/SiC counterpart, a higher temperature rise for the same amount of dissipated power. As detailed in previous works using this same technology [20], [21], [26], the maximum junction temperature limit directly affects the choice of the optimum load, strongly limiting the design space to a relatively small portion of the Smith chart close to maximum efficiency point. To conceive a space-compliant GaN/Si PA, the junction temperature must, thus, be regarded as a key parameter that may drive the designer toward different choices with respect to classical ones for terrestrial applications.

B. Devices' Thermal Model

As discussed in previous works [20], [26], a simplified nonlinear model proposed by the foundry has been adopted for the evaluation of the junction temperature (T_j). The formula, recalled here for convenience, is (all temperatures are in kelvin)

$$T_j = T_{BS} \cdot e^{\frac{R_{th,REF} \cdot P_{diss}}{T_{REF}}} \quad (1)$$

where T_{BS} is the backside temperature, P_{diss} is the dissipated power (more details follow), and T_{REF} is the temperature at which the reference thermal resistance $R_{th,REF}$ is computed (the foundry provides, for all allowed device peripheries, the $R_{th,REF}$ at 20 °C). The maximum allowed dissipated power P_{diss} computed with this formula is around 2.1 W/mm.

The dissipated power is obtained from CW LS (harmonic balance) simulations and computed as follows:

$$P_{diss} = P_{dc} + P_{in} - P_{out} = P_{dc} + P_{in}(1 - G_p) \quad (2)$$

where the input and output RF power should consider the sum of all harmonic components. Due to the relatively low power gain G_p achievable at very high frequency, especially for the larger transistors in the high-power stage, the input power is not negligible, hence contributing to device heating. However, the heating mechanism is different with respect to drain self-heating, since most of the input power is dissipated across the gate parasitics. To be conservative, in (2), we consider it as if it were totally dissipated in the active channel.

The adopted model has been verified by means of Raman measurements and 3-D electrothermal simulation with a finite-element solver [20].

C. Architecture and Device Selection

The selected architecture is a four-stage corporate amplifier configured in a 1:4:8:16 cascade, as depicted in Fig. 1. Following the rough estimation of halving the expected output power density when considering space-grade thermal limits, and accounting for the values reported in [15] and [24] (2.4 and 2.7 W/mm obtained at Ka-band) for terrestrial HPAs implemented with the same technology, a total periphery of 6.4 mm is selected in order to achieve the target power range. Considering then the available gain from different device peripheries at the target frequency, as well as MMIC dimension constraints, the final stage was implemented, combining in parallel 16 devices, each of 4×100-μm gate periphery. The combination of such a huge number of devices is not new in Ka-band [31], [32], but it clearly adds challenges to the output power combiner (OPC) design in terms of layout optimization, especially given a fixed chip size, load balance, combiner losses, and risk of oscillations, as well as electromagnetic (EM) crosstalk and thermal coupling.

To fit the MMIC dimensions, it was necessary to share source grounding via holes between adjacent devices to not exceed the given area: this increases via inductance and hampers thermal sinking, possibly increasing the transistor thermal resistance, since adjacent devices can be thermally coupled. To account for the latter effect, 3-D thermal simulations have been adopted to assess the effective thermal resistance of the transistors in the final stage, including, in the simulation, a preliminary layout of the matching networks around them. Indeed, the increase in the value of $R_{th,REF}$ to be considered in the final stage due to cross heating was simulated to be as high as 8% of the value for isolated devices with individual via holes.

Extensive CW load–pull simulations were carried out to find the optimum bias and load. According to space derating rules [22], the drain supply voltage is set to 11.25 V [21] in all simulations, while different gate voltages are explored, corresponding to the class-AB bias points from 15% down to 2.5% of the maximum current (about 1 mA/mm). As anticipated in Section II-A, the optimum load for the 4×100 μm device adopted in the final stage is mainly determined by the 160 °C temperature limit. As shown in Fig. 2, the optimum value is $\Gamma = 0.78\angle 141°$ for all the tested biases [21]. As can be noted, it sensibly differs from the optimum load for terrestrial applications, which is not allowed, as it would give a junction temperature above 160 °C at full power, and lies in a highly reflective region of the Smith chart, thus making the output combiner bandwidth and sensitivity to process variations particularly critical.

A deep class-AB bias current of 35 mA/mm, corresponding in simulation to a gate voltage of $V_G = -1.7$ V, was finally chosen, since, as detailed in Fig. 3, it allows for maximizing the available junction temperature swing versus input power and, hence, the achievable output power. Despite the relatively low small-signal (SS) gain associated with this bias point, device simulations show a sensible gain expansion with input power (nearly 2 dB), and hence, saturated PAE values are in line with those achievable at higher bias currents.

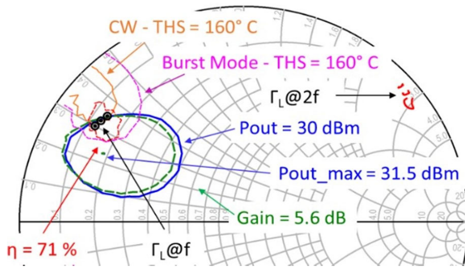


Fig. 2. Simulated load–pull contours of the 4 × 100-μm device at 36 GHz [21].

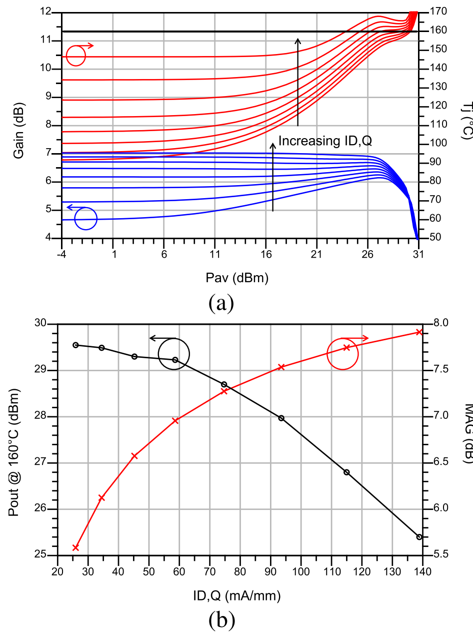


Fig. 3. Impact of junction temperature on bias point selection. (a) Simulated power gain and junction temperature versus input power at different biases. (b) Simulated maximum achievable output power and MAG versus quiescent current density.

Given a maximum available gain [MAG; see Fig. 3(b)] of around 6 dB for the final stage, three driver stages have then been added to achieve the target 20 dB of total gain. As detailed in Fig. 1, eight 4 × 75-μm devices are used for the last driver stage, while the second stage is composed of four 4 × 50-μm devices. Finally, a single 4 × 75-μm device completes the MMIC as the input stage. It is to highlight that the driver transistors have been deliberately oversized so as to ensure linearity and power driving capability margins to account for possible underestimation of the passive networks' losses, trading off with PAE.

D. Output Combiner and Matching Networks Design

Given the high number of devices in the final stage, the OPC and the last interstage matching networks are the most critical and challenging of the entire design. In particular, the main challenges are minimizing losses and sensitivity to process variations and presenting balanced loads to all the devices. The former goal is achieved by adopting the minimum number possible of lumped elements (MIM capacitors). Moreover, to minimize EM coupling effect, a relatively large structure with simple RF-shorted quarter-wavelength bias lines has been conceived, and a careful layout EM optimization was performed to achieve low losses and good matching.

However, despite the geometrical symmetry of the combiner, unequal load impedances (electrical asymmetry) were observed during the EM simulations. To balance the impedance levels at all drains, hence balancing and aligning their output voltages and currents, two straightforward methods have been proposed so far: shunt connections, as, for example, reported in [5], and geometrical symmetry unbalances, as, for example, reported in [33]. These two techniques can also be adopted jointly, as shown in [24], if necessary. In this design, only shunt connections have been adopted to force symmetrical operation of the final stage devices. Low-impedance shunts between all adjacent input ports of the combiner allow small differential currents to flow, thus obtaining uniform drain voltages and almost equal load impedances for all transistors (see Fig. 4). The magnitude of such differential-mode currents is evaluated through LS simulations so as to assess the feasibility of this solution (if the current is too high, geometrical asymmetry must be added to keep them under a reasonable limit) and to properly dimension the shunts.

The interstage matching between the driver and final stage implements a 2:4 device power splitting: the eight driver's transistors (4 × 75 μm) are coupled in pairs; then, each pair feeds four transistors of the final stage. Shunt connections are also added between the drains of the paired device. This choice provides lower losses and better compactness with respect to the more classical 1:2 device power splitting, adopted instead between the second and third stages. The interstage matching network between the first and second stages requires a 1:4 device power splitting, yielding a rather large impedance transformation, which has been addressed with multistep matching. At the gate side, all the interstage matching networks include RC stabilization, designed for wideband unconditional stability also at large dc drain currents, and odd-mode resistors to prevent differential-mode oscillations and force electrical symmetry as well. To keep the structures conceptually simple, all bias lines have been designed to be transparent in the operating band: at the gates, RF chokes (inductive meandered lines and/or spiral inductors) are used for this scope, while for the drains, the same result is achieved by connecting the dc-feed lines at short circuit points in the interstage matching networks. All bias voltages are provided from both the north and the south sides of the chip, yielding a fully symmetrical MMIC. Fig. 5 shows the simulated losses for all the matching networks and the input return loss of the MMIC, better than −20 dB in the design bandwidth.

Fig. 6 reports the final schematic of the MMIC. The simulated HPA achieves 19 dB of LS gain, which is considered satisfactory, and is capable to provide nearly 12 W with 29% PAE in the 35.5–36-GHz range, as shown in Fig. 7(a). The maximum junction temperature obtained in CW only slightly exceeds the 160 °C limit, as shown in Fig. 7(b), which is the satisfactory results considering the very conservative approach adopted in determining this value. Indeed, 3-D thermal simulations at 80 °C MMIC backside temperature performed on the final MMIC layout, adopting 116 thermal sources (one

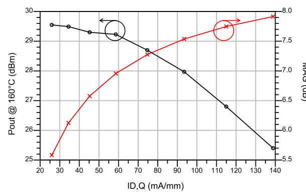


Fig. 4. Loads synthesized by the OPC (top 8 loads shown, and the bottom 8 are identical for symmetry) compared with target value (black cross) in the 34–37-GHz range.

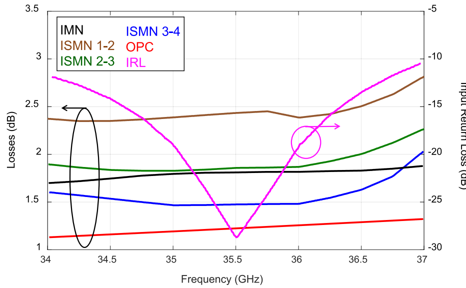


Fig. 5. Matching networks losses and PA input return loss.

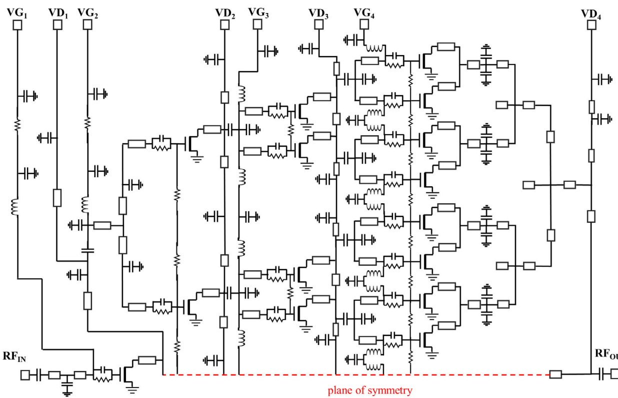
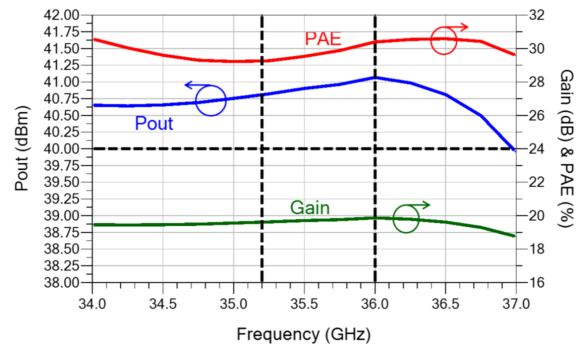


Fig. 6. Schematic of the MMIC HPA: as the circuit is fully symmetric, only one half of the circuit is shown.



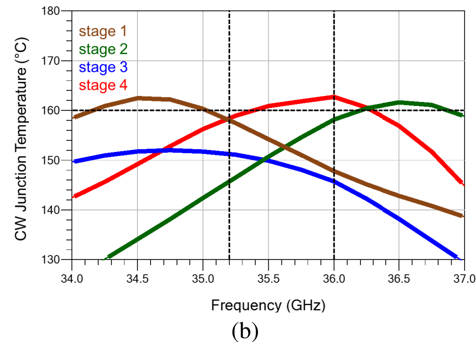


Fig. 7. CW simulation results in the 34–37-GHz range at 80 °C backside temperature and fixed input power (21.2 dBm). (a) Performance versus frequency [21]. (b) Transistors' junction temperatures according to (1).

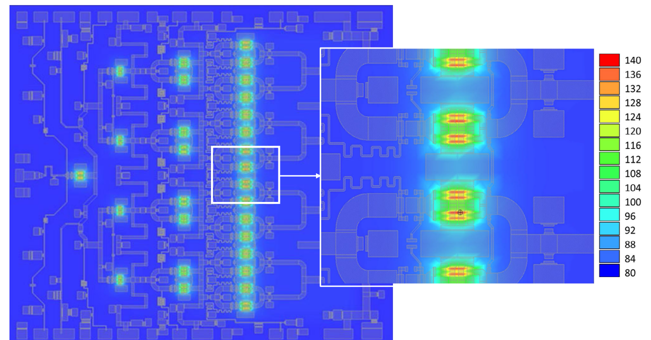


Fig. 8. Results of the 3-D thermal simulation of the final HPA.

per each transistor finger in the HPA), demonstrate that the maximum temperature should be only 140 °C, as reported in Fig. 8.

III. Measurements

The on-wafer characterization of all the available samples has been presented in [21], indicating very promising power performance, however accompanied by relatively low efficiency compared with simulations, and a large performance spread at the nominal biasing condition, due to the threshold voltage dispersion that prevented proper deep class-AB operation. After a further preliminary characterization with temporary (epoxy) mounting, a couple of chips were selected and assembled (by eutectic mounting) in their final test jig. In the following, the measurement setup and characterization results of the best chip will be presented, together with the test jig design.

A. Test Jig Design and Manufacturing

The mechanical structure of the designed test jig is illustrated in Fig. 9. The MMIC is mounted on a nickel/gold-plated copper carrier through the eutectic die attach technique (service provided by an external company). Copper has been selected to ensure good thermal properties (heat dissipation), while coating is essential for the eutectic brazing procedure. The eutectic layer is made of a 30-μm-thick Au80Sn20 alloy. X-rays inspection (Fig. 10) of both assemblies shows a void rate below 10%.

The RF board is attached to the carrier using an electrical conductive layer and thermal dissipative one. The center of the structure is milled to ensure the same height for the different parts to be connected with bonding wires. Additional aluminum elements were adopted to reinforce the mechanical strength of the thin RF substrate.

The RF board connects the MMIC to the external flanged 2.92-mm (K) coaxial connectors, which embed a glass-bead core. It has been designed on the RT/Duroid 6002 (PTFE Ceramic) substrate, which was (according to the information received at the time of the design from the manufacturer) fully qualified for space applications. A calibration (TRL) module

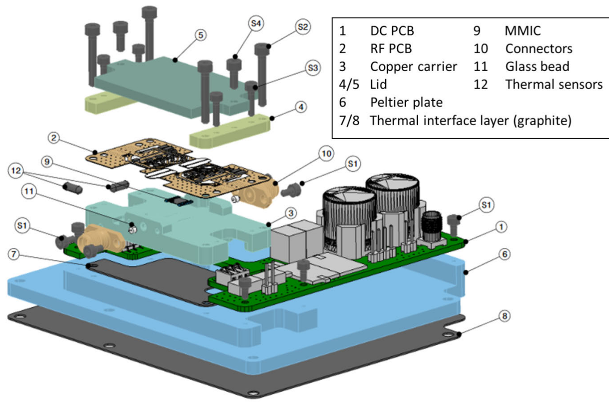


Fig. 9. Exploded-view drawing of the designed test jig.

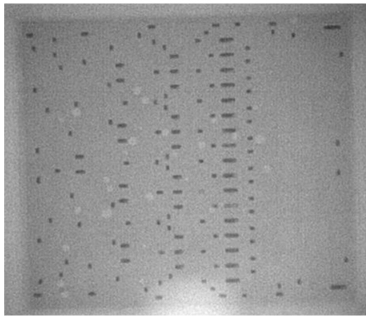
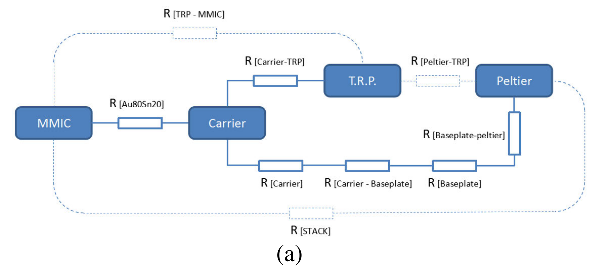
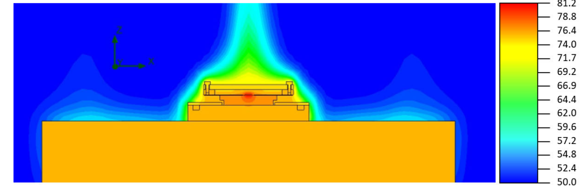


Fig. 10. X-ray inspection of the mounted chips.

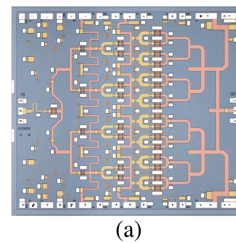


(a)

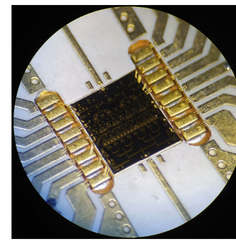


(b)

Fig. 11. Thermal simulation of the carrier. (a) Thermal stack-up. (b) Results at 75 °C Peltier and 50 °C ambient temperature.



(a)



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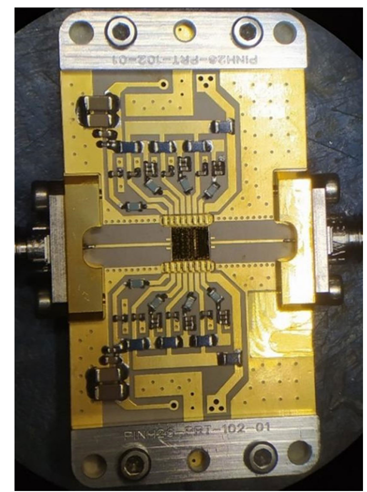


(c)

Fig. 12. Pictures of the assembled MMIC. (a) Bare MMIC. (b) Mounted chip. (c) Complete test jig.

on the same substrate has been designed and mounted on an identical carrier to de-embed the effect of the RF board from MMIC measurements.

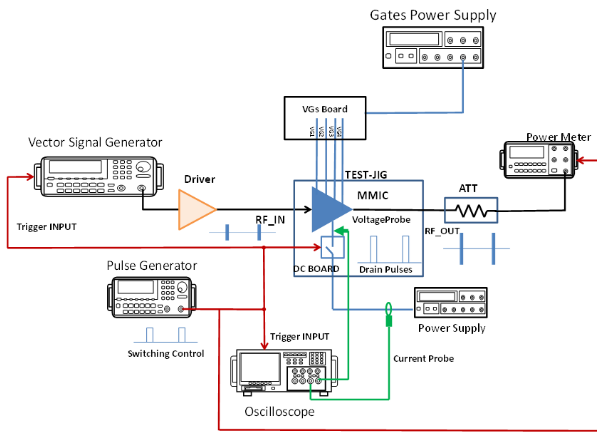
The dc board, made on a four-layer epoxy (FR4) PCB, was specifically designed to complete the dc bias network, partly integrated on the chip, with larger external capacitors up to 10 μF and to implement the fast-switching circuitry necessary for pulsed measurements. The turning on and off of the HPA are controlled through the drain voltage of all stages. This technique has been preferred over gate voltage switching to improve the efficiency and noise behavior of the system [34].

The carrier is then mounted on a Peltier plate to keep the backside temperature of the chip constant. The carrier–MMIC interface adopts a 5-mil graphite foil to ensure good thermal contact, spreading heat along the entire contact surface. Instead, a 10-mm aluminum plate serves as the interface between the Peltier module and the carrier. As it is not possible to measure the temperature right at the MMIC backside, a sensor is attached to the carrier, acting as temperature reference point (TRP). Extensive thermal simulations of the test jig were performed to optimize the TRP placing and to derive the relationship between the Peltier and MMIC backside temperatures, as shown in Fig. 11.

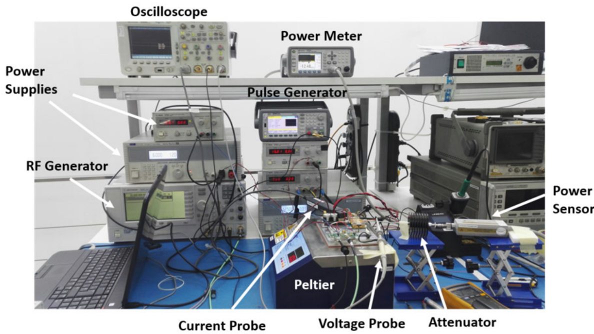
B. Measurement Setup

Fig. 12 shows the HPA assembled on the test jig. The module has been characterized both in SS and pulsed LS conditions at different controlled temperatures and drain voltages to check its performance under different operating conditions.

The *S*-parameters were measured by adopting a conventional CW setup with constant dc bias, while the dc/RF pulsed setup of Fig. 13 was used for power sweep characterization. The pulsed RF signal has an on-time equal to 120 μs and a period of 12 ms (1% duty cycle). The dc drain supply is also pulsed with an on-time of 130 μs, namely, 5 μs before and 5 μs after the RF signal, as detailed in Fig. 13(c). Rise and fall times of the dc pulse are within 20 ns; thus, the dc value can be considered fully stabilized after the 5-μs prebiasing margin adopted. To improve measurement accuracy, the dc pulse generator triggers all the measuring instruments as well as the RF generator. The drain current and voltage waveforms are captured with an oscilloscope, and their average value within the RF pulse is adopted to compute efficiency. Since the high current driven by the switching circuitry introduced considerable losses, a closed-loop control was added to ensure the desired voltage at drain terminals. For both SS and LS measurements, a higher quiescent current density (+45%) with respect to the nominal one considered in the simulation is adopted in all stages to guarantee that all devices are in conduction, to avoid the detrimental effect of threshold voltage spread observed with the on-wafer measurements [21].



(a)



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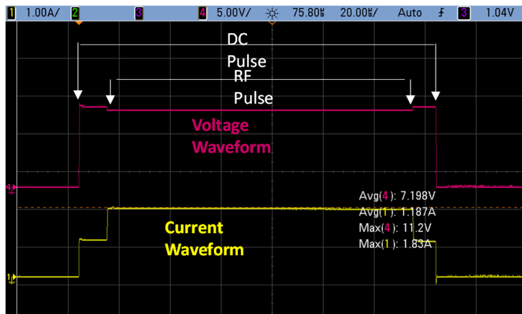


(c)

Fig. 13. Pulsed LS measurement setup. (a) Block diagram. (b) Picture. (c) Pulse waveforms on the oscilloscope.

C. Measurement Results

The results of the S-parameter characterization are shown in Fig. 14. Compared with simulations predictions with the same bias (i.e., increased to 50 mA/mm to avoid transistors in off state as previously said), a frequency shift downward of around 2 GHz is observed, as evidenced by the resonance of S_{11}, while gain is up to 5 dB higher in the 35.5–36-GHz range, and, in general, higher at all frequencies. Despite a larger resonant peak around 2 GHz (above 0 dB in measurement compared with −8 dB in simulation), the MMIC showed no low-frequency stability issues in the characterization campaign.

The results of the LS characterization are shown in Fig. 15. Although the achieved output power is lower (0.3–0.8 dB) than the predictions of the simulations, it is higher than 10.7 W in the entire frequency range, thus exceeding the original target of 10 W, along with the desired 20-dB gain: a result comparable

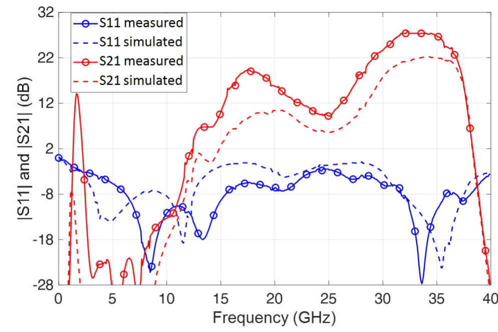


Fig. 14. SS results at 11.25 V, 50 mA/mm.

to the state of the at the target frequency, as reported in Table I. On the other hand, the measured efficiency is lower (ten points) than expected, which, in turn, implies a dissipated power higher than 45 W at full output power (peak value at 36 GHz). This value is 1.5 times the one predicted by simulations (30 W); hence, it is extremely critical from a thermal point of view. In fact, as shown in Section II, the maximum simulated CW channel temperature was around 162 °C at 80 °C backside: under the same conditions, assuming that the fraction of the total dissipated power actually dissipated in the final stage is the same as in simulation, the expected CW channel temperature from the measured dissipated power is as high as 208 °C, unacceptable for a space application. Although Fig. 8 shows that the predictions of the CW simulation are pessimistic, the calculated 208 °C value is too high to be considered safe. The discrepancy between simulations and measurements is confirmed by the power sweep results shown in Fig. 16(a): beyond the lower saturated power and efficiency, the gain expansion predicted by simulations is not found in measurements. A device model update was released by the foundry in the meantime, and resimulating the HPA, the discrepancy between simulation and measurement results was sensibly reduced, as demonstrated in Fig. 16(b): the new model is indeed able to predict the relatively poorer efficiency found during the MMIC characterization, which can be ascribed to short-channel effects, leading to a critical threshold voltage control/uniformity in the wafer. Such effects can be neglected when the dc operating point of the active devices is far enough away from pinch-off (a condition where, in fact, the model update produces no significant changes), but are evident in the presented design due to the choice of a very deep class-AB bias, aimed at enhancing saturation efficiency and power density.

In order to reduce the dissipated power and find an optimum space-compliant operating point, the MMIC was then characterized at lower drain voltage values, namely, 10 V (11% reduction) and 9 V (20% reduction of the supply voltage). Fig. 17 shows that at an SS level, the use of a lower drain voltage has no effect, while in Fig. 18, the results obtained in pulsed LS characterization are reported. The designed HPA is capable of providing 8.4 and 6.6 W at 10 and 9 V, respectively, in both cases with the same 20-dB gain and 19% PAE achieved at the nominal drain voltage (11.25 V), but with the maximum dissipated power reduced to 37 W at 10 V and to 30.5 W at 9 V. The latter value, same as

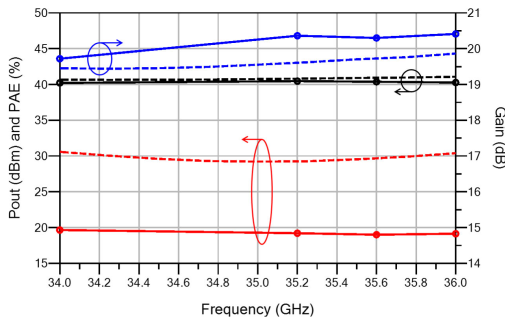


Fig. 15. Pulsed LS measurement results (circles) at fixed input power (18.1 dBm) with 11.25-V, 50-mA/mm bias compared with simulations (dashed lines): output power (black), gain (blue), and PAE (red).

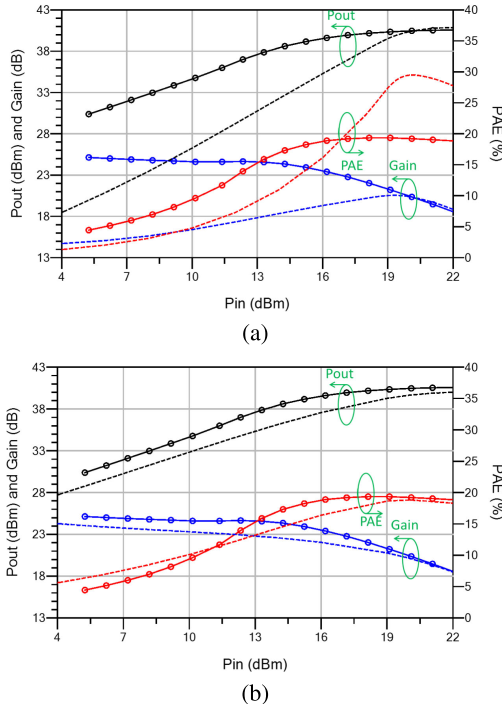


Fig. 16. Power sweep at 35.2 GHz with 11.25-V, 50-mA/mm bias: comparison between measurements (circles) and simulations (dashed lines). (a) Device model adopted in the design. (b) Updated foundry device model.

in the original simulations, is expected to bring a maximum junction temperature well within the 160 °C thermal limit at an 80 °C MMIC backside temperature, hence assuring that the HPA biased at 9 V can be considered space-compliant. At this bias, the MMIC achieved a still noticeable output power of 6.6 W, corresponding to an output power density of 1 W/mm. As shown in Table I, compared with the work in [19], adopting the same technology but working under shallow class-AB bias where the stability issues encountered in this design are mitigated, the achieved space-compliant output power density and efficiency can be considered as state of the art for GaN/Si technology. Compared with GaN/SiC counterparts, it clearly suffers from the poor thermal properties of the Si substrate when space-grade constraints are considered.

Because of the good results achieved at 9 V, the HPA was fully characterized at this bias, including distortion characterization, shown in Fig. 19, measurement over temperature, and performance at the actual operation conditions with SAR input signals, reported in the following paragraphs.

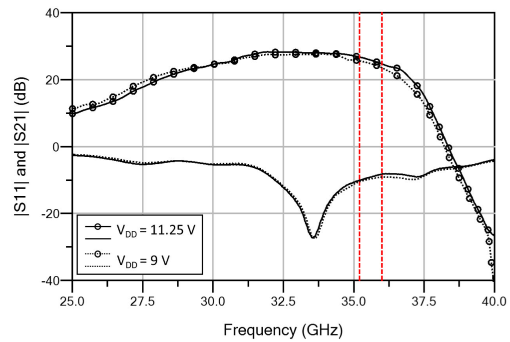


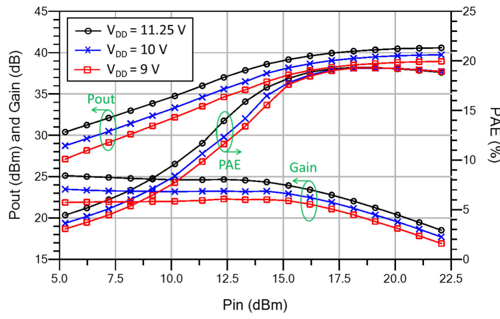
Fig. 17. S_{11} (no symbols) and S_{21} (circles) of Sample 1 at two different drain voltages.

D. Characterization in Temperature at 9 V

The HPA was characterized at −10 °C and 80 °C in both SS and LS conditions. The performance of the HPA in temperature is extremely stable in both SS and LS conditions. The S-parameter characterization showed nearly no variations in the return loss and around 1-dB SS gain difference between the coldest (−10 °C) and hottest temperature (80 °C), as shown in Fig. 20. The LS characterization was performed from 34 to 36 GHz (the characterization band was extended toward lower values according to the observed shift with respect to simulations) and for two different values of the duty cycle, namely, 1% and 30%, corresponding to an on-time of 120 μs and 3.6 ms, respectively (maintaining the pulse period of 12 ms). This comparison is intended to observe how the larger on-time (more than 20 times the dominant thermal time constant of the largest devices) impacts on performance. The results are reported in Fig. 21. The worst case output power variation with temperature for the 1% duty cycle case was as low as 0.0029 dB/°C, while efficiency was practically the same at the two temperatures. For the 30% duty cycle measurements, the effect of temperature is only slightly more pronounced, with a worst case output power variation with a temperature of 0.0041 dB/°C and a PAE drop of nearly 0.4 points. Compared with state-of-the-art GaN/SiC commercial products [35], [36], showing variations in the 0.02–0.033-dB/° range and up to five points of PAE variation over 60 °C temperature variation, it is clear that the thermal sensitivity of this GaN/Si technology is a key strength over GaN/SiC counterparts.

E. Characterization in SAR Mode at 9 V

The HPA was finally characterized with an SAR modulated signal from 34 to 36 GHz, to assess pulse-to-pulse (P2P) amplitude and phase stability, two important parameters for radar applications [37], in a real-scenario operation. The input signals are generated in the baseband and then upconverted with a vector signal generator, adopting 500-MHz linear chirp bandwidth. Both the interleaved mode, with concurrent RF + dc pulses, and the closed-burst mode, keeping dc power on for a number of consecutive RF pulses forming a burst [23], were tested. Note that in the interleaved mode, dc pulses may be critical for stability due to trapping effects, typically pronounced in GaN technologies [38], [39]. On the other hand, the closed-burst scenario suffers from thermal effects, affecting also P2P stability [40].



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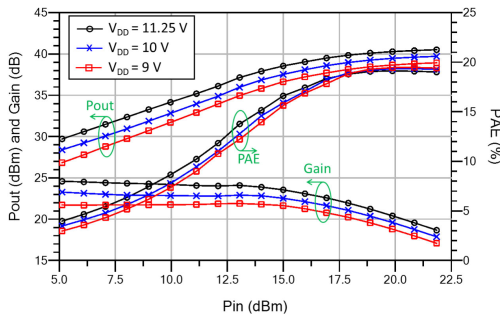

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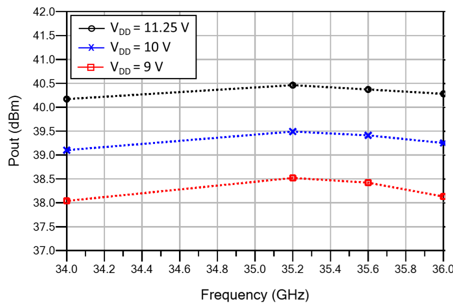

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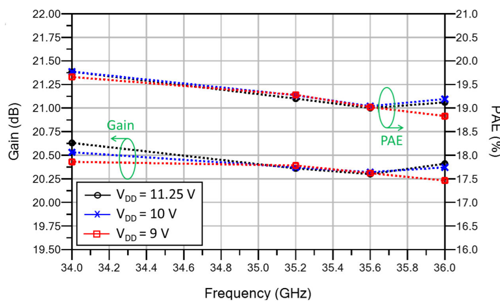


(d)

Fig. 18. LS characterization at different supply voltages. (a) Power sweep at 35.2 GHz. (b) Power sweep at 36 GHz. (c) Output power in the 34–36-GHz range. (d) Gain and PAE in the 34–36-GHz range.

In particular, four different test cases have been considered: two interleaved modes with different pulse duration and duty cycles (d.c.), namely, 12 μs with 20% d.c. (IM1) and 18 μs with 30% d.c. (IM2), and two closed-burst modes with 64 (CB1) and 16 (CB2) 49-μs-long pulses per burst, corresponding, with the 12-ms burst period, to a dc duty cycle of 30% and 10%, respectively. For the SAR-mode characterization, the HPA was biased at 9 V to ensure reliability, especially considering the 30% burst duty cycle case, while the backside temperature is fixed at the hottest value of 80 °C. The

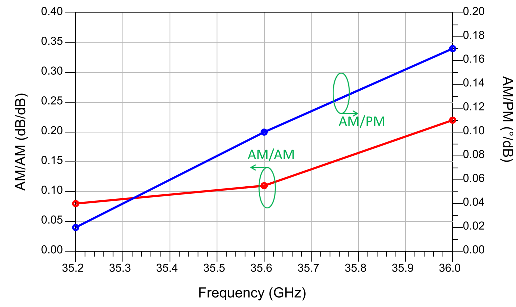


Fig. 19. Measured AM/AM and AM/PM at 38.2-dBm output power (9-V bias).

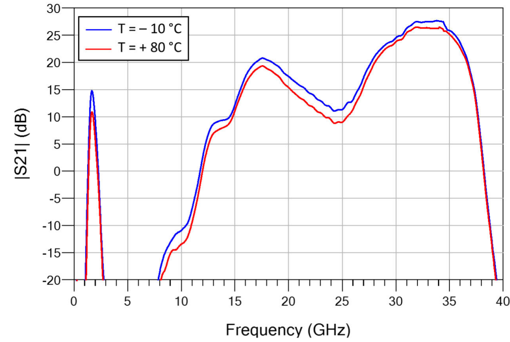
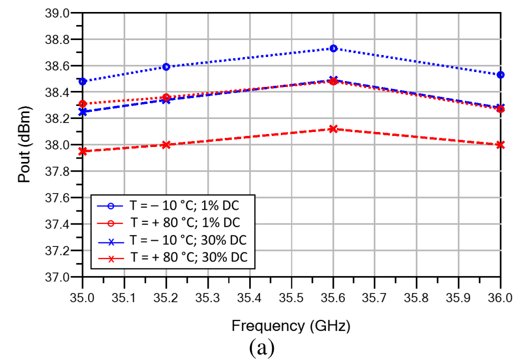
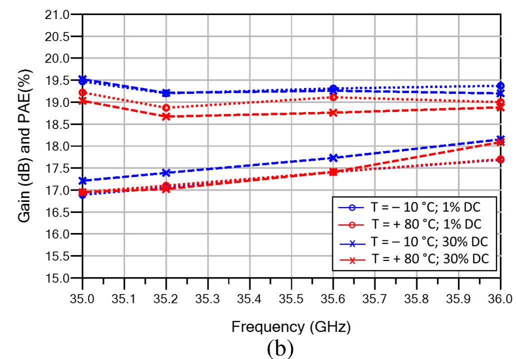


Fig. 20. SS gain at different temperatures.



(a)



(b)

Fig. 21. LS characterization at different temperatures. (a) Output power. (b) Gain and PAE.

amplitude (S_A) and phase (S_P) P2P stability were computed from the amplitude and phase standard deviations (σ) as follows [37]:

$$S_A = 10 \cdot \log_{10}\left(\frac{\sigma_A^2}{\overline{A}^2}\right) \tag{3}$$

$$S_P = 10 \cdot \log_{10}(\sigma_P^2) \tag{4}$$

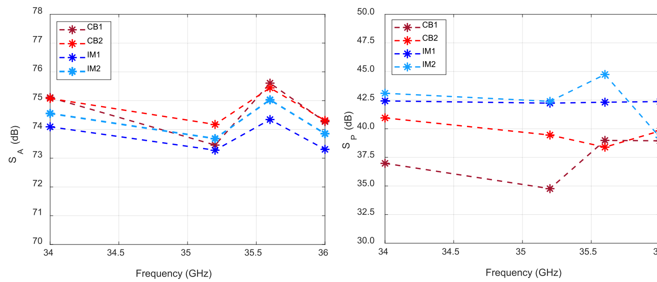


Fig. 22. P2P stability with SAR modulated signal characterization results at 9 V, 80 °C.

where $\overline{A}$ is the average value of the pulse amplitude. The results are shown in Fig. 22. For CB signals, the burst-to-burst statistics are obtained considering a test sequence of five bursts, while for IM signals, the P2P characteristics are taken from ten sequential pulses.

The obtained amplitude stability is remarkable, being in the 75-dB range in all cases, while concerning phase, variations up to 1° were observed, yielding to phase stability in the 35–45-dB range. These results can be considered very satisfying. Note that most of the experimental results available in the literature are at S-band [37], [38], [40], [41]; thus, a direct comparison would not be totally fair, as the achievable phase measurement accuracy at Ka-band is not comparable to what is attainable at S-band, even when resorting to high-end instrumentation equipment.

IV. Conclusion

In this work, we reported the detailed design and full characterization of a Ka-band power amplifier designed for space SAR altimeter applications. Due to a critical bias choice for the adopted technology, which, in turn, lead to inaccurate simulation results, the designed HPA achieved in measurement a PAE lower than expected at the target output power, in excess of 10 W, and a gain of around 20 dB. Nonetheless, considering a 20% reduction of the supply voltage, corresponding to 1.8-dB output power decrease, the designed HPA is capable of providing 6.6 W, with the same gain and PAE, by keeping the maximum junction temperature of the devices within the 160 °C limit posed by space derating, which is in line with the state of the art for a GaN/Si space-grade amplifier.

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Maria Del Rocìo Garcìa, photograph and biography not available at the time of publication.

Iain Davies, photograph and biography not available at the time of publication.

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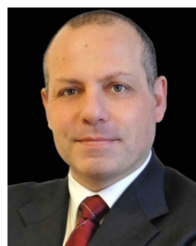

Paolo Colantonio (Fellow, IEEE) received the degree in electronics engineering and the Ph.D. in microelectronics and telecommunications from Università Degli Studi di Roma, Tor Vergata, Rome, in 1994 and 2000, respectively.

He is currently a Full Professor of microwave electronics with Università Degli Studi di Roma. He is the author or co-author of more than 300 scientific articles. He authored the book *High Efficiency RF and Microwave Solid State Power Amplifiers* (Wiley, 2009), three book chapters, four contributions to the *Encyclopedia on Microwave Electronics* (Wiley), and one international patent. His research activities are mainly focused on the field of microwave and millimeter-wave electronic devices and, in particular, on the design criteria for nonlinear microwave subsystems and high-efficiency power amplifiers.

Dr. Colantonio was elevated to the grade of an IEEE Fellow for the contribution to microwave power amplifiers in 2024. He has been the Chair of EuMIC 2022. He is an Associate Editor of IEEE MICROWAVE AND WIRELESS LETTERS.

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