A New Hardware/Software Platform and a New 1/E Neutron Source for Soft Error Studies: Testing FPGAs at the ISIS Facility

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***Abstract*—We introduce a new hardware/software platform for testing SRAM-based FPGAs under heavy-ion and neutron beams, capable of tracing the bit-flips in the configuration memory back to the physical resources affected in the FPGA. The validation was performed using, for the first time, the neutron source at the RAL-ISIS facility. The ISIS beam features a 1/E spectrum, which is similar to the terrestrial one with an acceleration between 10^7 and 10^8 in the energy range 10–100 MeV. The results gathered on Xilinx SRAM-based FPGAs are discussed in terms of cross section and circuit-level modifications.**

***Index Terms*—FPGA, neutron source, radiation testing, Single Event Upset (SEU).**

I. Introduction

SOFT ERRORS (SE) are a concern for electronics reliability and dependability not only in the space environment, but also at sea-level, due to neutrons originating from the interactions of cosmic rays with the atmosphere and to alpha-emitting contaminants in the package/solder materials [1]–[3]. Radiation-induced errors may be particularly severe in SRAM-based FPGAs, where modifications in the configuration memory (known as bit-flips) may alter the implemented circuits [4]–[9]. Assessing the SE cross-section is the first necessary step to evaluate the device sensitivity to radiation. Unfortunately, knowing the cross section of the configuration memory is not enough to carefully understand the SE impact on the application functionality, since each bit maps a different function inside the FPGA architecture.

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The contribution of this paper is twofold. Firstly, we introduce a new European facility for neutron irradiation, proving for the first time the suitability for SE testing of the ISIS neutron source (Didcot, U.K), used so far for solid state physics studies. Only few dedicated facilities exist providing neutron beams matching the terrestrial flux, such as the LANSCE, TRIUMF, and RCNP sources [10]–[12]. The ISIS neutron beam features an energy spectrum that is similar to the terrestrial one with an acceleration factor between 10^7 and 10^8, making it appropriate for accelerated tests of sea-level electronic applications, as demonstrated in the test runs performed on July 18–20, 2006. Accelerated tests must always be checked against life-testing as pointed out in various contributions [13]–[15], but this kind of facilities is a powerful instrument and is strongly needed, especially in Europe.

Secondly, the new platform we present in this paper offers designers the capability of measuring cross sections both for the configuration memory and the implemented circuits. Furthermore, by post-processing the experimental data, we can obtain information on the exact modifications induced by the radiation. In particular, it is possible to analyze the content of the FPGA memory elements to identify where SEUs occur, detecting what type of resources are affected (logic resources, routing resources, or user memory resources), and assessing the impact on the circuit implemented by the FPGA.

II. The ISIS Facility

The ISIS neutron source is located at the CCLRC Rutherford Appleton Laboratory (Didcot, U.K.) and has been used so far for condensed matter studies. Neutrons are produced at ISIS by the spallation process [16]: a heavy-metal target (tungsten) is bombarded with pulses of highly energetic protons, generating neutrons from the nuclei of the target atoms. The acceleration process is composed of two steps: first H^- ions are injected into a linear accelerator (LINAC). The beam is converted to protons by a 0.3 μm thick aluminum oxide stripping foil and then accelerated in a synchrotron. The high-energy proton pulses finally strike the tungsten target and corresponding pulses of neutrons are freed by spallation. The energy of the produced neutrons is reduced through a moderator, which can be of different types. Further details on ISIS can be found in [17]. The resulting neutron beam reaches 26 different lines (Fig. 1), including the VESUVIO line where our experiments were performed. VESUVIO is commonly employed for condensed matter studies, exploiting neutrons above 1 eV, the so-called epithermal neutrons. The sample S is located at

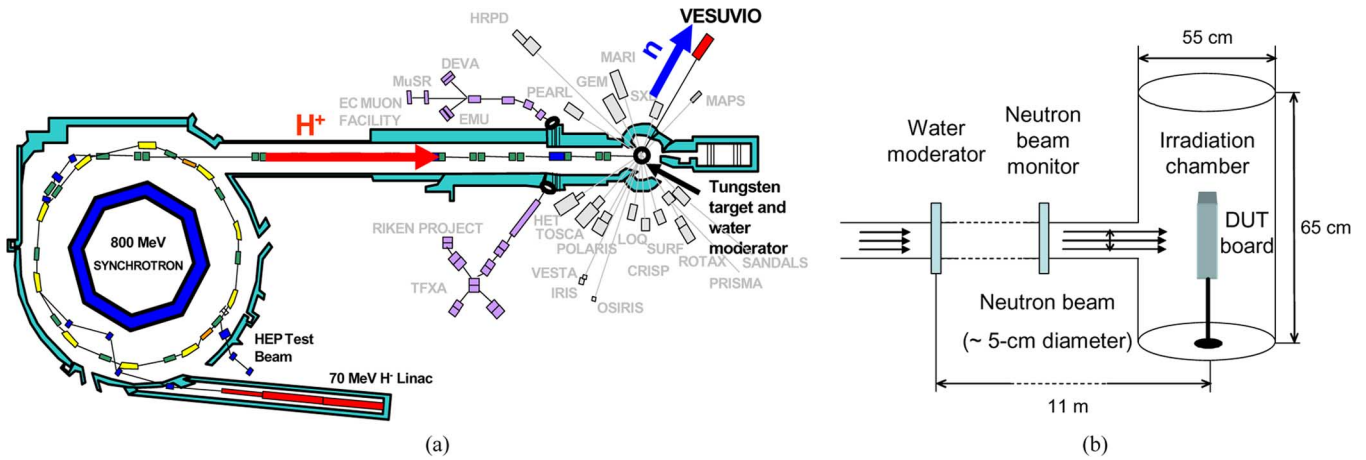

Fig. 1. Schematic of (a) ISIS neutron facility and (b) VESUVIO irradiation chamber.

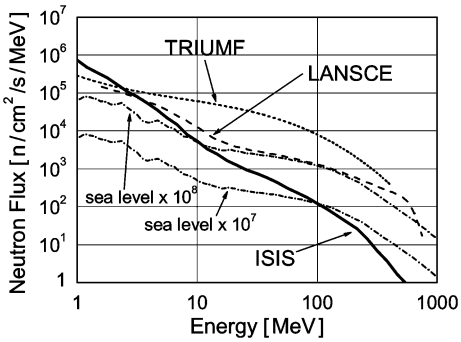

Fig. 2. ISIS spectrum compared to those of the LANSCE and TRIUMF facilities and to the terrestrial one at sea level multiplied by 10^7 and 10^8.

a distance $L_0 = 11.055$ m from the water moderator. The Aluminum sample tank is of cylindrical form, with an internal diameter of 50 cm. The height is 65 cm and the beam center is located at about 30 cm from the top. The spectrum in the high-energy region has been measured through the threshold activation target technique [18]. The ISIS spectrum is illustrated in Fig. 2, where it is compared with two of the most widely used neutron sources (LANSCE and TRIUMF) and with the terrestrial flux multiplied by a factor of 10^7 and 10^8. As seen, the ISIS spectrum features a $1/E^{\alpha}$ characteristic, with α larger than one, and provides a flux similar to the terrestrial one with acceleration between 10^7 and 10^8 in the energy range 10–100 MeV. The ISIS spectrum integrated above 10 MeV yields $7.86 \cdot 10^4\ \mathrm{n \cdot cm^{-2} \cdot s^{-1}}$ on the irradiated device.

Studies have been made to compare ISIS to other spallation neutron sources through the use of the charge-coupled device (CCD) sensor described in [19]. Differences in the neutron spectrum of the ISIS source with respect to LANSCE result in different charge collection spectra in the CCD. A "LANSCE equivalent flux" [20], i.e., the effectiveness of ISIS neutrons in producing events in the CCD compared to LANSCE ones, has been measured yielding a value of $6.7 \cdot 10^4\ \mathrm{n \cdot cm^{-2} \cdot s^{-1}}$. The equivalence is based on the number of events measured with the CCD above a certain threshold (417 ke). In other words, if we divide the number of events in the CCD sensor collected in the ISIS and LANSCE beams by the LANSCE-equivalent flux, we obtain the same event cross section.

III. Background

The purpose of this section is to introduce the readers to the architecture of FPGAs, as well as to provide insights as to the possible effects of SEs affecting the FPGA configuration memory.

A. An Introduction to FPGAs

An FPGA consists of an array of logic blocks that can be selectively interconnected to implement different designs. An FPGA logic block is typically capable of implementing many different combinational and sequential logic functions. An FPGA routing architecture incorporates wire segments of various lengths that can be interconnected via electrically programmable switches. The distribution of the length of the wire segments affects directly the density and performance achieved by an FPGA.

The SRAM-based FPGA generic model used in this work is shown in Fig. 3. This architecture is used by several families of SRAM-based FPGAs [21], [22]. The model consists of three kinds of resources: *wiring segments*, *logic blocks*, and *switch boxes*.

Wiring segments are chunks of wiring devoted to transferring information among logic blocks. Wiring segments are organized in the horizontal plane traversing an FPGA from east to west, and the vertical plane traversing the FPGA from north to south. Wiring segments are used in conjunction with switch boxes to deliver information between any locations inside FPGAs.

Logic blocks contain the combinational and sequential logic components required to implement the user circuit, which is defined by writing the proper bitstream inside the FPGA configuration memory. As an example, a simple logic block can contain a Look Up Table (LUT) to implement combinational functions, a flip-flop (FF) to implement memory elements, and multiplexers (MUX) for implementing different signal forwarding strategies. Each logic block has a number of input and output signals connected to adjacent switch boxes and logic blocks through wiring segments. The SRAM programming technology uses static RAM cells to control pass gates or multiplexers.

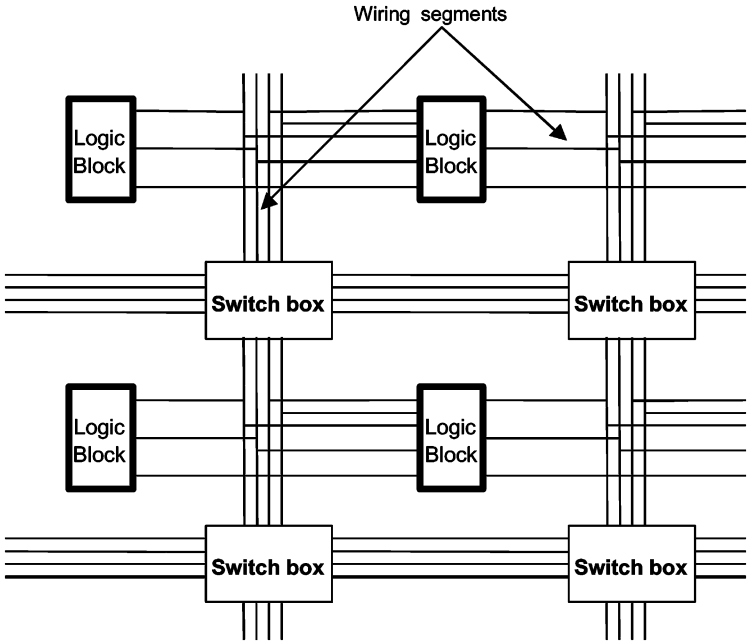

Fig. 3. Generic FPGA architecture model.

The programmable interconnection network consists of wiring segments that can be connected or disconnected by several programmable interconnect points (PIPs) organized to form *switch matrices*. PIPs (also called routing segments) provide configurable connections between pairs of wiring segments. The basic PIP structure consists of a pass transistor controlled by a configuration memory bit. There are several types of PIPs: *cross-point PIPs* that connect wire segments located in disjoint planes (one in the horizontal plane and one in the vertical plane), *break-point PIPs* that connect wire segments in the same plane, and *compound PIPs* which consist of a combination of n cross-point PIPs and m break-point PIPs, each controlled separately by groups of configuration bits. There are also *Decoded Multiplexer PIPs* which are groups of 2^k cross-point PIPs sharing common output wire segments controlled by k configuration memory bits. Conversely, *non-decoded MUX PIPs* consist in k wire segments controlled by k configuration bits.

B. Effects of SE On FPGA Resources

All the above-mentioned resources are controlled by the *configuration memory*, which is a set of storage elements (either implemented using SRAM or Flash technology) placed inside the FPGA device. The content of the configuration memory defines how wiring segments, logic blocks, and switch boxes are used for implementing a given circuit. A SE affecting such a memory may have a dramatic impact, since it may change the functionality of the circuit.

Although they do not induce permanent modifications to the hardware, when SEs occur in the FPGA configuration memory they may alter the implemented circuit, until new configuration data are written. The errors produced by SEs in the FPGA configuration memory (Single Event Upset or SEU) can be classified in two different categories: errors that affect logic blocks and errors that affect switch boxes [23].

As far as logic-block errors are concerned, several different phenomena may be observed, depending on which logic block resource was modified by a SEU.

1. *LUT error*: the SEU modified one bit of a LUT, thus changing the combinational function it implements.
2. *MUX error*: the SEU modified the configuration of a MUX in the logic block; as a result, signals are not correctly forwarded inside the logic block.
3. *FF error*: the SEU modified the configuration of a FF, for example changing the polarity of the reset line, or that of the clock line.

As far as switch boxes are concerned, different phenomena are possible. Although a SEU affecting a switch box modifies the configuration of only one PIP, both *single* and *multiple* effects can be originated.

Single effects happen when the modifications induced by the SEU only alter the affected PIP. In this case one situation may happen, which we call *open*: the SEU changes the configuration of the affected PIP in such a way that the existing connection between two routing segments is opened.

In order to describe the multiple effects, let us consider the two PIPs A_S/A_D and B_S/B_D connecting the end-points A_S, A_D, B_S, B_D, as shown in Fig. 4(a). We identified the following modifications that could be introduced by a SEU.

1. *Short* between A_S/A_D and B_D/B_S. As shown in Fig. 4(b), a third PIP connecting either one end of A to one end of B is enabled. This can happen if A_S/A_D and B_S/B_D belong to the same switch box, and the SEU modifies the configuration memory bit related on the compound PIP that connects B with A.
2. *Open*, which corresponds to the opening of both PIPs A_S/A_D and B_S/B_D, as shown in Fig. 4(c). This situation may happen if a SEU modifies a configuration memory bit belonging to a decoded PIP group and controlling both A_S/A_D and B_S/B_D.

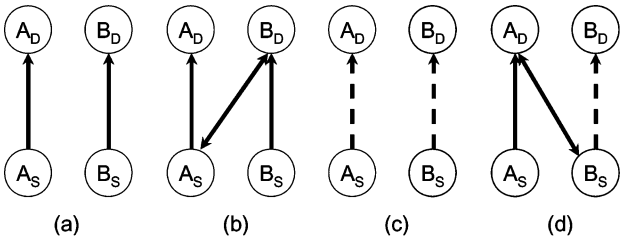

Fig. 4. Possible multiple effects induced by one SEU: (a) normal condition, (b) short between B_D and B_S, (c) open, (d) open short.

3. *Open/Short*, which corresponds to the opening of either the PIP A_S/A_D or the B_S/B_D one, and to the enabling of the PIP A_S/B_D or B_S/A_D, as shown in Fig. 4(d). This situation may happen if a SEU modifies a configuration memory bit belonging to a decoded PIP and controlling both A_S/A_D and B_S/B_D.

The short effects, as shown in Fig. 4(b), may occur if two nets are routed on the same switch box and a new PIP is added between them. This kind of faulty effect effectively happens when a cross-point PIP, which is non-buffered and has bi-directional capability, links two wire segments located in disjoint planes. Conversely, the Open and the Open/Short effects, as shown in Fig. 4(c) and (d), may happen if two nets are routed using decoded PIPs.

IV. The Developed Platform

The hardware/software platform we developed aims at supporting designers in validating system implemented using SRAM-based FPGAs. It offers three functionalities.

1. *Static test*: the DUT configuration memory is initialized to a known pattern. Then, during radiation exposure, the DUT memory is periodically read and compared with the expected pattern. This functionality is used to measure the device *static cross section*, defined as the ratio between the number of SEUs and the fluence of hitting particles. Through the static cross section designers quantify the sensitivity of the *FPGA technology* to a specific radiation source.
2. *Dynamic test*: the DUT configuration memory is initialized to a user-defined circuit. The DUT is submitted to a set of user-defined stimuli and the outputs are constantly read and compared with the expected ones. In case of mismatch, the content of the DUT configuration memory is read and compared with the expected one. This functionality is used to measure the device *dynamic cross section*, defined as the ratio between the number of SEUs producing a wrong output and the fluence of hitting particles. Through the dynamic cross section, designers quantify the sensitivity of the *FPGA implemented circuit* to any specific radiation source.
3. *Circuit-level post-processing*: the faulty configuration memories recorded during either static or dynamic testing are analyzed. The analysis consists of the following.
   a. Identifying which type of resource was affected: logic blocks or switch boxes;
   b. Identifying the resource that was affected: which logic block, and which programmable interconnect point (PIP) within a switch box;
   c. Identifying which part of the user-defined circuit was affected (in case of dynamic testing): which logic block, and which PIPs within a switch box that implement the user circuit.

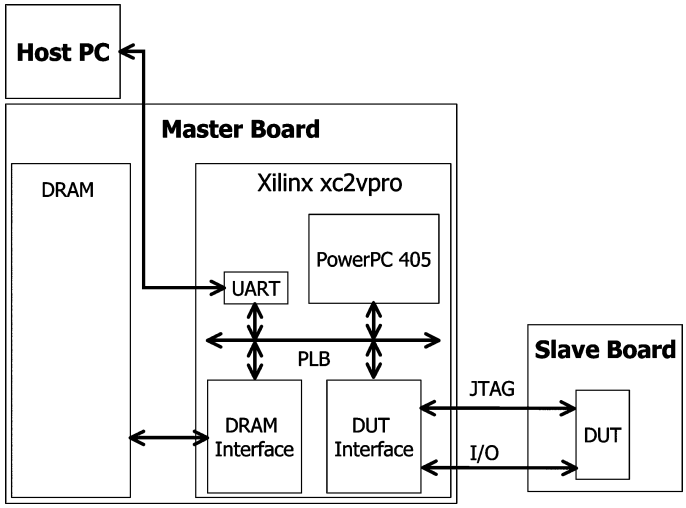

Fig. 5. The developed hardware/software platform.

The main contribution of the platform is the possibility of relating SEUs in the FPGA memory with the user circuit implemented by the FPGA, thus allowing very detailed debugging of the performance of the error detection, masking, and correction features the circuit employs.

The architecture of the developed platform is outlined in Fig. 5. The main components consist of the following.

1. *Host PC*: it is a personal computer used for data logging during testing, and for circuit-level post-processing.
2. *Mother Board*: it is a board equipped with a Xilinx Virtex 2 Pro device, and 256 MBytes of DRAM memory. The mother board is the core of our system, and it is in charge of executing all the operations needed for the testing:
   - downloading the configuration memory to the DUT;
   - applying the input stimuli to the DUT;
   - reading the content of the DUT memory;
   - reading the DUT output.

   The Virtex 2 Pro device implements these functionalities partly in software (on the PowerPC 405 the FPGA embeds) and partly in hardware. In particular, all the operations needed for supervising the execution of the above-mentioned operations are executed in software, while suitable hardware components are used for communicating with the Host PC, the DRAM memory, and the DUT.
3. *Daughter Board*: it is a board where the DUT is mounted.

V. Circuit-Level Post-Processing

The circuit-level post-processing consists in analyzing the content of the FPGA configuration memory collected during radiation testing and in identifying the modifications induced by SEUs to the resources of the FPGA. These analyses are performed through the CIrcuit-Level ANalysis TOol (CILANTO)

[8], which exploits a database where the relationship between the FPGA resources and the configuration memory bits is described.

We used CILANTO to perform a bit-by-bit comparison between the *reference* FPGA configuration memory (i.e., the one stored in the FPGA device before the occurrence of any SEU) with the *faulty* configuration memory collected during radiation testing. For each bit of the faulty configuration memory that differs from the reference one, CILANTO lists the corresponding FPGA resource (logic block or switch box). In particular, in case of logic blocks, CILANTO is able to identify whether the SEU hits a LUT, a MUX or a FF. In case of switch boxes, CILANTO reports the information about the affected PIPs showing the type of modification that the SEU originated and the names of the circuit interconnections that use the PIPs involved in the modification.

CILANTO implements an important feature that consists in identifying those bits of the FPGA configuration memory that are sensitive for a given user-circuit the FPGA implements. They include those bits whose value must be defined for configuring the FPGA resources in such a way that the FPGA implements the user circuit, and those bits that are not used by the user circuit, but that may have side effects on the user circuit when altered by SEUs.

VI. Experimental Results

We performed a set of radiation testing experiments with the ISIS neutrons on the 18–20 July, 2006, in order to validate the platform we developed, irradiating a SRAM-based FPGA (Xilinx Spartan-3 xc3s200 [25]). This device has a configuration memory of 1,047,616 SRAM cells that control a matrix of 480 CLBs organized in a matrix of 24 rows and 20 columns. This device is particularly suitable for our purpose since it is widely used for automotive applications [25].

1. When performing an initial static test, we computed the static cross section reported in Table I. Cross sections are computed using both the actual flux at ISIS ($7.86 \cdot 10^4$ n/cm^2/s) and the "LANSCE equivalent" flux ($6.7 \cdot 10^4$ n/cm^2/s). These results are a good indication of the correctness of the platform we developed, since they are consistent with the accelerated testing performed at Los Alamos Neutron Science Center and presented in [9].
2. We then performed the dynamic test on an elliptic filter working on a set of 32 samples, and we analyzed the gathered results by exploiting the circuit-level post-processing feature our platform includes. The circuit was selected as a representative of those data-processing applications that may benefit from being implemented through SRAM-based FPGAs. Being the configuration memory of the adopted FPGA sensitive to SE, we adopted the Xilinx Triple Module Redundancy (XTMR) hardening technique to protect it [24]. XTMR consists in the triplication of all inputs, combinational logic, and routing. All inputs, outputs, and voters are replicated three times (each replica is known as TMR *domain*), and thus these resources are no longer a single points of failure, and the result is potentially immune from upsets provoking a single effect in the voting circuitry. To ensure constant synchronization between redundant state machines, XTMR inserts majority voters on all feedback paths. As a result, the feedback logic for each state machine is a function of the current state of all three state machines. If a single error provoked by a SEU occurs in combinational logic or in a state machine, one of the replicas of the circuit behaves differently from the others. For this reason, in absence of radiation-hardened voting circuits (as in the case of Virtex or Spartan-3 Xilinx families) XTMR protects voting logic from SEUs by replicating three times the voters and by adding circuitry that detects the replica that is behaving differently and disables it by placing its pin in a high-impedance state while the other two replicas continue to operate correctly and drive the correct outputs.
3. We applied CILANTO to the FPGA configuration memory of the elliptic filter design hardened by the X-TMR tool and it identifies an amount of 75,016 configuration memory bits used by the implemented elliptic filter. Secondly we used CILANTO on the several faulty FPGA configuration data memory recorded during the radiation experiment. From this analysis CILANTO identifies only 19 configuration memory bits that have been upset during the whole dynamic test and none of these bitflips affects the correct functionality of the implemented elliptic filter. In particular, we observed that among the 19 bitflips, 17 are related to configuration memory bits that control resources not used by the implemented circuit, while only 2 bitflips are related to resources that effectively map the elliptic filter functionality. The report produced by CILANTO identifies that the effects are related to interconnection PIPs of a unique TMR domain. In particular, CILANTO identifies two short effects related to elliptic filter nets belonging only to the second domain of the TMR, thus they do not corrupt the TMR circuit functionality.

TABLE I
Static Cross Section

#Run	ISIS Fluence [n cm^{-2}]	LANSCE Equivalent Fluence [n cm^{-2}]	ISIS Cross-Section [cm^2]	LANSCE Equivalent Cross-Section [cm^2]
1	$2.76 \cdot 10^8$	$2.35 \cdot 10^8$	$2.98 \cdot 10^{-14}$	$3.50 \cdot 10^{-14}$
2	$2.74 \cdot 10^8$	$2.34 \cdot 10^8$	$3.75 \cdot 10^{-14}$	$4.40 \cdot 10^{-14}$
3	$2.76 \cdot 10^8$	$2.35 \cdot 10^8$	$3.35 \cdot 10^{-14}$	$3.93 \cdot 10^{-14}$
4	$2.76 \cdot 10^8$	$2.36 \cdot 10^8$	$2.23 \cdot 10^{-14}$	$2.62 \cdot 10^{-14}$
5	$2.76 \cdot 10^8$	$2.35 \cdot 10^8$	$1.86 \cdot 10^{-14}$	$2.19 \cdot 10^{-14}$
6	$2.76 \cdot 10^8$	$2.35 \cdot 10^8$	$1.86 \cdot 10^{-14}$	$2.19 \cdot 10^{-14}$
7	$2.65 \cdot 10^8$	$2.26 \cdot 10^8$	$3.50 \cdot 10^{-14}$	$4.10 \cdot 10^{-14}$
8	$2.76 \cdot 10^8$	$2.35 \cdot 10^8$	$2.98 \cdot 10^{-14}$	$3.50 \cdot 10^{-14}$
Overall	$\mathbf{2.20 \cdot 10^9}$	$\mathbf{1.87 \cdot 10^9}$	$\mathbf{2.81 \cdot 10^{-14}}$	$\mathbf{3.30 \cdot 10^{-14}}$

VII. Conclusions

We introduced a new hardware/software platform for testing FPGAs under heavy-ion and neutron beams. The validation of the platform was performed on July 2006 using, for the first

time, the 1/E neutron beam source at the RAL-ISIS facility. The ISIS beam presents characteristics useful for performing accelerated single event testing of electronics components, emulating the sea-level terrestrial neutron spectrum and fluence with an acceleration between 10^7 and 10^8. The static and dynamic testing of Xilinx FPGAs was discussed in terms of cross section and circuit-level modifications induced on an elliptic filter hardened through the X-TMR tool.

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