An Ultra-Wideband Monolithic Active Balun

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***Abstract*— An integrated active Balun has been developed for ultra-wideband communication systems. This solution integrates in a single chip a protection from the presence of high-level signals, an ultra-wideband amplifier, a further differential-to-single ended amplification stage and an impedance transformer. The MMIC has a very large bandwidth ranging from 0.5 GHz to 18.0 GHz and has been conceived to be driven by a self-complementary antenna and a balanced mode with an input impedance of 150 ohms. In addition, the circuit has a single bias from the output port that greatly simplifies the mechanical structure of the module. Performance are promising, having measurements confirmed the simulation results.**

Keywords—Active Balun, MMIC, ultra-wideband circuits.

I. Introduction

Many Ultra-WideBand Electronic Warfare (UWB EW) systems work in the band (0.5-18.0) GHz. Such multi-octave systems often require a critical design of RF components and circuits. For instance, one of the key issues for UWB EW systems is the realization of directional antennas for a multi-octave bandwidth. To this purpose, a planar self-complementary antenna design approach has demonstrated significant performances and the antennas are usually fabricated on thin printed circuit boards, with very low losses. An absolute gain of 0-5 dBi is achieved with a directional radiation pattern. The antenna provides a differential, balanced mode signal with an output impedance of 60π ohms; while the output signal of the antenna requires RF front-ends with an input overload protection, a broadband Balun, an amplification stage and a high impedance driver with minimized group delays.

For UWB applications several broadband amplifiers have been reported in the literature, but they usually have a non-zero common mode amplification and so an additional Balun is necessary to drive differential mode antennas [1]. In addition, generally, a passive Balun has very large size, introduce losses and is not suitable to operate in a large bandwidth. The impedance transformer composed of discrete, passive components for the microwave frequency range requires a large size as well. Overload protection is also mandatory before the low-noise amplifier, and this is usually implemented as a separate chip or hybrid circuit, with additional losses and space occupation. To solve these issues, we have integrated the four functions necessary to match the receiver to the UWB radiating element into a single chip. The UWB microwave limiter, the low noise amplifier, the balanced to single-ended adapter and the impedance transformer are all included in the MMIC in a compact solution. In addition, the further feature of a single DC feeding has also included in the design. This allows to obtain a high integration factor with a consequent reduction of costs and sizes. The MMIC has been defined and fabricated using the model library of a commercial GaAs pHEMT foundry. The MMIC has a bandwidth from 0.5 GHz to 18.0 GHz with 14 dB gain, 4.5dB NF, better than 20 dB common-mode rejection and 30 dBm input overload protection. Both simulations and measurements results are in good agreement, demonstrating the feasibility of the proposed solution and its reliability to be used in practical applications.

II. Technology and System Architecture

The technology chosen for the design is the 0.15 μm Power PHEMT 3MI from Qorvo foundry, with transition frequency at 80 GHz, as a good compromise between gain, linearity and noise. Unfortunately, no low-resistance/low-capacitance/high-current diodes are available in this technology and they could be useful for the power limiter design. So, gate diodes have been used to this purpose, in a suitable arrangement as shown in the next Section.

At system level, the architecture of the active Balun has been optimized in order to have a compact design in integrated technology, even embedding all the functionality previously described, and also providing the capability to furnish the DC bias from the MMIC RF output port, so significantly enhancing also the mechanical design of the receiver and the feeding architecture. Also at circuital level, the proposed solution inherits some design choices typical of different kind of applications to realize the Balun function. In fact, the balanced-to-unbalanced conversion is here implemented with a differential amplifier that is the normal approach in Si circuits [2-7], but up to now it has been only occasionally used at microwave frequencies with GaAs-based technology [8-9], that exhibits better noise and linearity performances. In a previous work targeted to radioastronomy applications [2], for instance, low-noise performance has been obtained at the expenses of input match and using an off-chip input matching circuitry. The bandwidth was also limited compared to what is required for UWB electronic warfare. Obviously, no input protection was included, and also the bias scheme was

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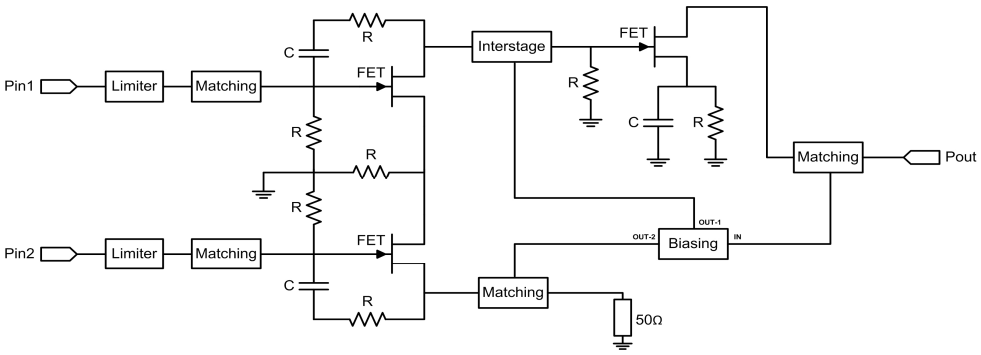

Fig. 1. Simplified schematic of the active Balun.

straightforward, making use of an independent bias line for each of the four transistors of the two-stage differential amplifier.

III. Active Balun Design

The general scheme of the active Balun is shown in Fig.1. The core of the MMIC is composed of a differential amplifier, followed by a single-ended common-source gain stage and preceded by two limiters, inserted in the two arms of the differential input. The limiters are realized with several GaAs gate diodes in parallel, shunting the access lines (Fig. 2a). The number of gate diodes, whose dimensions are 2x20 um, has been set in such a way that the maximum allowed current is not exceeded. It allows to protect the circuitry located downstream in the Balun when the antenna receives large incoming signals up to 30 dBm in the operative bandwidth. Contrariwise, the impact of the limiters on the performances of the Balun for low-level signals is negligible.

The following differential amplifier is able to furnish common-mode rejection and differential gain. The transistors are 4x25 μm devices; they are biased with a gate-source voltage of -0.7 V and a slightly different drain-source voltage (1.8 / 2.3 V). This is necessary since the transistors have different loads to implement the Balun function. The drain current is about the same for both the transistors and equal to 8 mA. A resistance between the coupled sources node and ground serves both for self-biasing and for common-mode rejection. The gate terminals are DC grounded by means of additional large resistors. An RC-series feedback branch has been also added between drain and gate in order to improve the input match, improve the stability characteristics and reduce the noise figure of the circuit. The matching networks include both lumped elements (capacitances, inductances and resistors) and transmission lines. A CMRR better than 20 dB has been obtained by careful design and optimization of the networks even if the differential stage has an unbalanced output. In fact, one of its output is connected to 50 Ohm, while the other one is connected to an interstage matching network followed by a second single-ended amplifier in common source configuration. The transistor in the second stage makes use of a self-biasing architecture with a source resistor shunted by a large capacitor. The FET is a 4x50 μm device, biased with a gate-source voltage of -0.55 V and a drain current of 18 mA useful to increase the dynamic range of the circuit, providing a high compression point.

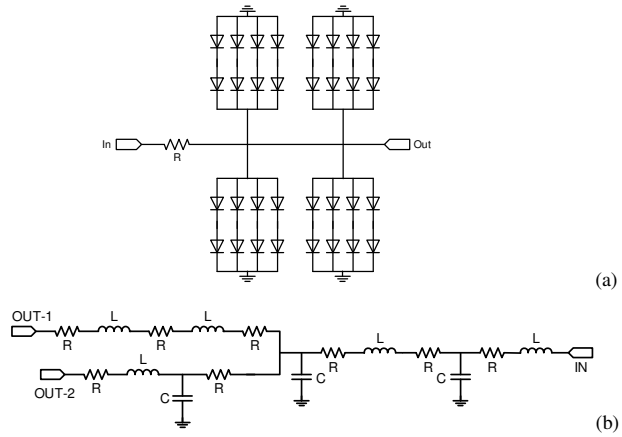

Fig. 2. Simplified architecture of the limiter (a) and of the bias network (b).

A critical section of the design has been the bias network, whose simplified schematic is reported in Fig.2b. In fact, the circuit has been conceived with a single bias voltage (6 V) that must be applied from the RF output port of the MMIC and have to reach both the amplification stages considered in the system. This implies that some closed-loop feedback paths are present in the circuit and so the bias circuitry has been carefully designed avoiding possible instability concerns. A low-pass network topology has been adopted to this purpose, making use of a distributed series of resistors, large inductances and grounded capacitances useful to provide an effective RF ground. The bias network has also been used for the improvement of the performances of the amplification stages at the lower frequencies [11].

IV. Results and Measurements

The active Balun here proposed has been fabricated by Qorvo foundry; the chip dimensions are 2x4 mm. It has been glued in a test jig provided of SMA connectors and access microstrip lines (Fig. 3). With a different jig and also an integrated antenna the chip has been already evaluated in [11]. Here, the MMIC has been measured by means of a three-port Vector Network Analyzer, for calibrated S-parameter measurements with a balanced input and single-ended output. The Vector Network Analyzer Keysight PNA-X N5242A (10

MHz – 26.5 GHz) has been used for this purpose and the test bench is shown in Fig. 4. The balanced device (the active Balun) is designed to receive input simultaneously across two ports. Usually, standard balanced measurements apply stimulus to one port at a time, measures the responses, and calculates the theoretical balanced responses. While the option iTMSA (Integrated True Mode Stimulus Application) that has been considered, makes use the two PNA-X sources to apply either truly differential (180 degree out-of-phase) or truly common (in-phase) signals across the input of the balanced device. PNA receivers measure the single-ended response at the output of the device and calculate the balanced response.

The measured results are in good agreement with simulations. The effect of connectors, access lines and bonding wires have been also de-embedded from the measurements. In fact, preliminary simulations with an EM numerical solver had indicated that their effect could be responsible for at least part of the discrepancies between simulation and measurements. Performances are close to the expected ones: an average gain of 14 dB with a maximum return loss of 10 dB have been measured. The input return loss of the balanced mode is measured on a 150 Ohm reference impedance, while the output return loss is measured on a 50 Ohm reference impedance. The common-mode rejection is better than 20dB in most of the frequency band. The noise figure has an average value of 4.5 dB across the whole frequency band. Nonlinear measurements have been also carried out and they have shown that the input power at 1dB gain compression is greater than -1 dBm for most of the frequency band, that is, very close to specifications. Also the power consumption matches the simulation, with a total current of 35 mA at 6 V, for 20 mW total power consumption. Table I summarizes the main measured performance.

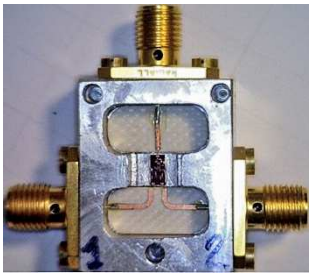

Fig. 3. Photograph of the chip mounted in the test jig.

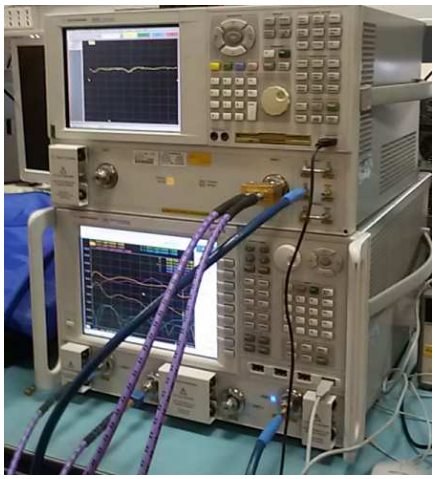

Fig. 4. Test bench with the measured results on the displays.

TABLE I. MEASURED PERFORMANCE

Parameters	**Value**
Frequency range (GHz)	0.5-18
Gain (dB)	14
Noise figure (dB)	4.5
Input matching (dB)	< -10
Output matching (dB)	< -10
P1dB input compression point	> -1

V. CONCLUSIONS

In this work we have proposed the design of an innovative 0.5-18 GHz GaAs active Balun, with integrated active protection against strong interfering RF signals. Measurements of the prototype show good agreement with simulations. This innovative solution allows easy integration of differential antennas directly with active device, without the need of large-size passive circuitry.

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