Experimental Results Obtained on a New Circuit Topology of a Broadband and Low Spurious Frequency Doubler

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***Abstract*—The performances of a frequency doubler based on a distributed amplifier are evaluated experimentally. The gate and drain artificial transmission lines have band-pass filter frequency behavior, centered on the fundamental and second harmonic, respectively. The circuit topology of this frequency doubler makes possible a significant reduction of the power level for the output fundamental and third harmonics. The frequency doubler characterized in this paper has the experimental values of the conversion loss less than 4 dB and 7 dB, when the input power level is equal to -1 dBm and 5 dBm, respectively, for the input frequency ranging between 4 GHz and 6 GHz.**

***Keywords*—frequency doubler; distributed topology; artificial transmission lines.**

1. Introduction

Broadband frequency multipliers are frequently used in communication and measurement equipments. In particular, hybrid or monolithically integrated broadband frequency doublers have been designed and fabricated, using Schottky diodes or transistors [1–5]. In [1], a GaAs Schottky diodes based frequency doubler having the conversion loss below 22 dB for input power level of 18 dBm has been reported for output frequencies from 50 to 110 GHz. Using heterojunction bipolar transistors, the conversion gain is possible for a low input power level between -30 and -15 dBm, and, moreover, high rejection of the output fundamental harmonic up to 28 dB are also possible, even up to 110 GHz [2]. Based on the Gilbert cell [3], similar performances as in [2] have been reported in [4] and [5], for frequencies up to 110 GHz and for frequencies from 36 to 80 GHz, respectively.

In [6], a new circuit topology for a broadband and low spurious distributed frequency multiplier has been analyzed and designed. In this paper, the experimental results for the frequency doubler proposed in [6] are presented and compared with the simulated ones. For clarity, the results obtained in this reference are reviewed shortly in the following. The schematic of this proposed circuit is shown in Fig. 1. The frequency multiplier is based on a distributed amplifier working under nonlinear regime. The gate and drain artificial lines consist of cascaded band-pass filters having the working frequencies equal to f_{in} and mf_{in}, respectively, when m is an integer number equal to the order of the frequency multiplication. If b_g and b_d are the phase shifts of the band-pass filters used to realize the gate and drain artificial lines (computed at the frequencies f_{in} and mf_{in}, respectively), the output power on the frequency harmonic mf_{in} is maximized if $mb_g = b_d$ (the *phase matching condition*) [6]. The fully-distributed topologies presented in Fig. 2 have been proposed to realize the gate and drain band-pass filters for a frequency doubler ($m = 2$), where θ_g and θ_d are equal to 180^0 at the central frequencies of these filters, $f_{0,in}$ and $2f_{0,in}$, respectively. In particular, the drain band-pass filter is composed of two identical cascaded cells, each one having the same circuit topology as for the gate band-pass filter. In this case, the expressions for the gate and drain phase shifts may be written as $b_g = \pi f_{in} / f_{0,in} + A$ and $b_d = 2\pi f_{in} / f_{0,in} + 2 \cdot A$, when $A = \sin^{-1}\left[(Z_c / Z_{c2}) \tan(\pi f_{in} / f_{0,in}) \right]$. From these formulas, it is observed that the phase matching condition is fulfilled for any frequency inside the pass-band of the gate and drain filters. These fully-distributed phase shifters have the same physical length. Taking into account the practical aspects related to the implementation of the distributed amplifier, this is an important advantage of using fully-distributed circuit topologies for the gate and drain phase shifters. This advantage is not available if fully-lumped

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band-pass filters are used. Indeed, if the drain band-pass filter is composed of two identical fully-lumped cascaded cells, each one having the same circuit topology as for the gate band-pass filter, the phase matching condition may be fulfilled over a large frequency bandwidth, but the physical lengths of the gate and drain band-pass filers differ significantly. For equal physical length, one cell may be used to realize the gate and drain band-pass filters, but, in this case, the phase matching condition may be fulfilled at the central working frequency, only.

Using fully-distributed circuit topology for the band-pass filters, a frequency doubler has been designed and fabricated for 4–6 GHz input frequencies, on RT/duroid 5870 substrate of 0.508 mm thickness [6]. For the gate and drain band-pass filters (see Fig. 2), $Z_{c2}=60\Omega$, $Z_{cx}=92\Omega$ and $Z_{cy}=110\Omega$ [6]. The characteristic impedance of these band-pass filters is $Z_c=50\Omega$, at the input central working frequency equal to 5 GHz.

The photograph of the realized circuit is presented in Fig. 3.

2. Description of the simulated and experimental conditions

InGaAs HEMTs have been used to realize the circuit. For the simulated results, the transistors have been modeled using the Angelov nonlinear equivalent [7]. Accordingly to this model, the drain current is: $I_d=I_{pk}\left[1+\tanh(\Psi)\right]\cdot\cdot\left(1+\lambda V_d\right)\cdot\tanh\left(\alpha V_d\right)$, where $\Psi=P_1V_{gr}+$ $+P_2V_{gr}^2+P_3V_{gr}^3$ and $V_{gr}=V_g+B_1\left(V_d-V_{db}\right)+$ $+B_2\left(V_d-V_{db}\right)^2-V_{pk}$. The parameters for the expression of the nonlinear drain current have been obtained in order to fit the DC characteristics of the transistor. It was obtained [8]: $I_{pk}=20\,\text{mA}$, $P_1=4.2$, $P_2=0.3478$, $P_3=0.0105$, $B_1=0.04$, $B_2=0$, $V_{db}=1\,\text{V}$, $V_{pk}=-0.11\,\text{V}$, $\alpha=4$ and $\lambda=0.12$, while V_g and V_d are the gate and drain voltages.

The bias point of the transistor have been imposed (in simulation and experiment) for the drain current and voltage equal to 10mA (the gate DC voltage is -0.3 V) and 1.5V, respectively.

The other parameters of the nonlinear equivalent circuit used in simulation have been obtained in order to fit, as well as possible, the scattering parameters of the transistor, up to 18 GHz, for the particular bias point specified above. The following values have been obtained for a unilateral equivalent circuit: $C_{gso}=0.36\text{pF}$ (gate-source capacitance), $R_i=20\Omega$ (intrinsic resistance), $C_{ds}=0.1\text{pF}$ (drain-source capacitance), $R_{ds}=1800\Omega$ (drain-source resistance), $\tau=0.006\text{ns}$ (gate-drain time delay), $L_g=0.58\text{nH}$ (gate inductance) and $L_d=1.05\text{nH}$ (drain inductance). The other parameters of the model have been neglected.

The frequency doubler has been simulated by means of the MWO software package [9].

The power level on the output harmonics have been measured using Anritsu MS2668C spectrum analyzer connected to the output of the circuit, while the Agilent E8257D signal generator has been connected to the input.

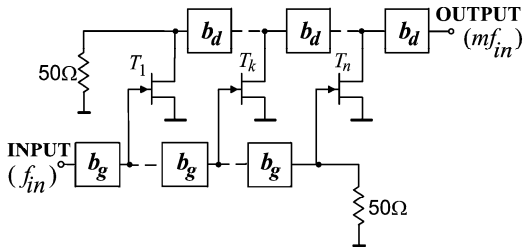

Fig. 1. Schematic of the distributed frequency multiplier.

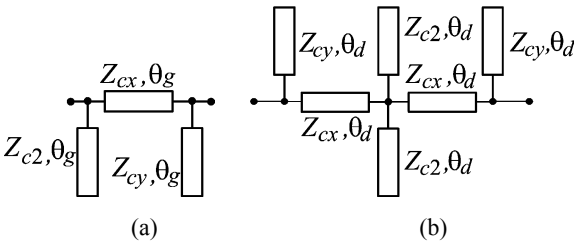

Fig. 2. Fully-distributed gate (a) and drain (b) band-pass filers used for the proposed frequency doubler.

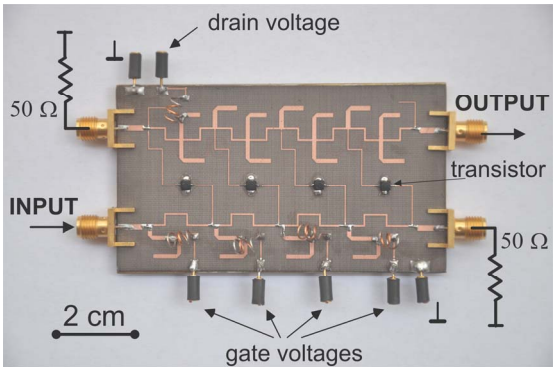

Fig. 3. The realized distributed frequency doubler.

The input and output return losses have been measured under small-signal condition using a scalar network analyzer.

3. Comparison between simulated and experimental results

The simulated results obtained with MWO and the experimental results for the output power on the first three harmonics versus the input frequency are shown in Fig. 4, for two input power level of -1dBm and 5dBm. As it can be observed, the output first and third harmonics are well filtered for input frequencies between 4 GHz and 6 GHz. For this frequency bandwidth, the output power level on the second harmonic has low variation.

The experimental values for the conversion loss on the second harmonic, for input frequency ranging between 4 GHz and 6 GHz, are less than 4 dB and 7 dB, for input power level of -1 dBm and 5 dBm, respectively.

The rejection at the output of the fundamental and third harmonics is more than 30 dB for both input power levels of -1 dBm and 5 dBm, for input frequencies between 4.5 and 5.5 GHz. These values decrease when the input frequencies approach the limits of the frequency bandwidth extended from 4 to 6 GHz, but they are higher than 10 dB for both the fundamental and third harmonics.

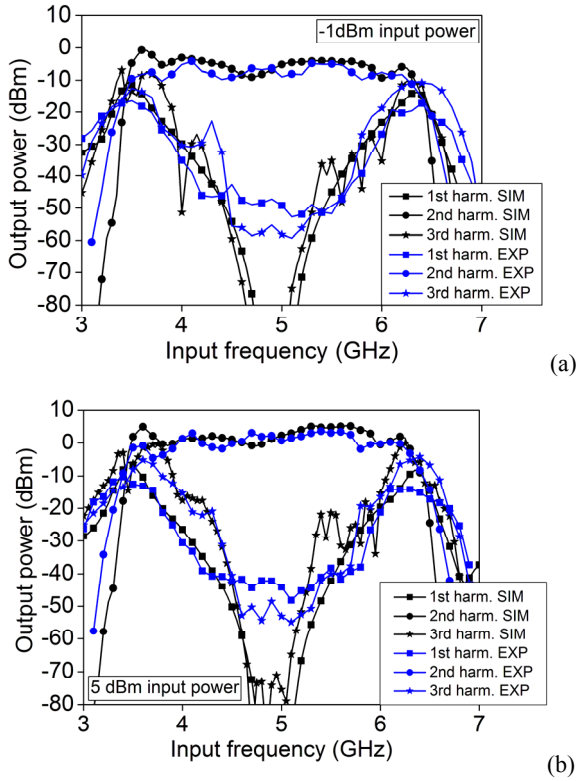

Fig. 4. Simulated and experimental output power level for the first three harmonics versus the input frequency, when the input power level is equal to -1 dBm (a) and 5 dBm (b).

The experimental results for the conversion loss versus the input power level are plotted in Fig. 5, for the input frequency of 5.6 GHz. From this figure, minimum values for the conversion losses are obtained for the input power level between 5 dBm and 9 dBm, when conversion losses of less than 1 dB are possible.

Fig. 6 presents frequency variation for the small-signal input and output magnitudes of S_{11} and S_{22}. It is observed that good impedance matching is obtained for input frequencies between 4 and 6 GHz, as well as for the output second harmonic between 8 and 12 GHz. The experimental values for the input and output return-loss are greater than 10 dB, for the input frequency range between 4 GHz and 6 GHz.

Conclusions

A frequency doubler based on distributed amplifier has been characterized experimentally.

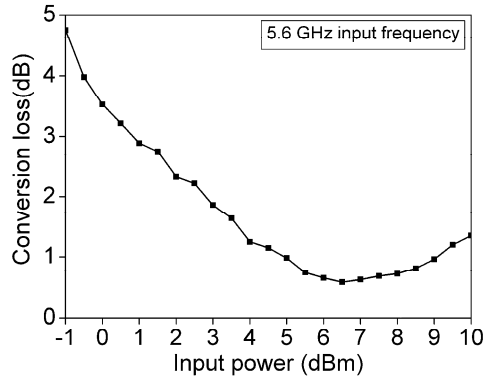

Fig. 5. Experimental conversion loss on the second harmonic versus the input power level, for the input frequency of 5.6 GHz.

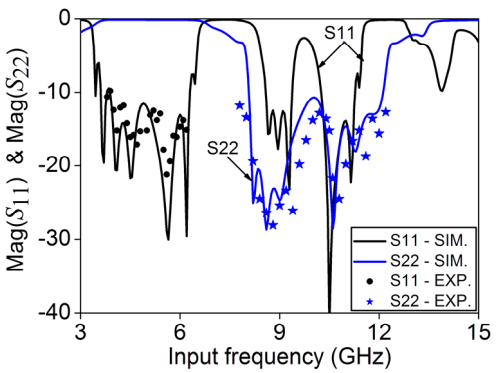

Fig. 6. Simulated and experimental input and output small-signal reflection coefficients.

For the analyzed frequency doubler, it has been demonstrated that low spurious output spectrum is possible if fully-distributed band-pass filters are used to realize the gate and drain artificial lines. The experimental output power values on the first three harmonics show a good agreement with the simulated ones.

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[9] AWR Microwave Office (MWO) software package – Applied Wave Research Inc.