Racetrack logic

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A building block for computing in memory systems is introduced. Based on the previously introduced racetrack memory proposed by IBM, a racetrack memory is used not only to store data but also to perform bitwise majority-based computations by coupling the memory with inputs provided by controllable magnets. This solution is defined as racetrack logic. Micromagnetic simulations are used to confirm that the proposed solution is technically viable.

Introduction: It is well known that the current pervasive diffusion of computing systems has been enabled by the continuous reduction of the dimensions of computing devices, which also enabled lower power consumption and higher performances. This reduction is coming to an end. Several emerging technologies are being explored both for memory and logic implementations none based on conventional CMOS technology.

Among the emerging technologies IBM researchers proposed magnetic racetrack memory, a new class of potential non-volatile storage-class memories [1]. It is based on the controlled motion of a series of domain walls along magnetic nanowires using spin-polarised current pulses. The objective of this Letter is to propose a novel device, based on racetrack memories, able also to perform logic functions and thus moving towards a 'computing in memory' paradigm. Differently from previous literature, for example [2], the storage elements are directly performing the logic functions. The rest of the Letter is organised as follows: first a background section will introduce the racetrack memory functional paradigm, and then we will show the proposed architecture for 'racetrack logic' and provide the simulation results. Finally, we will summarise the architecture's features with an equivalent circuit and draw some conclusions.

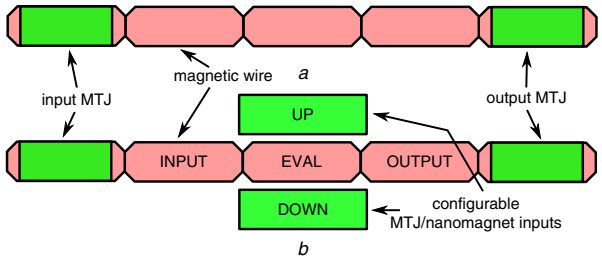

Fig. 1 *Basic structures*

a Racetrack memory. Ferromagnetic wire is used to store information. Notches are used to separate logic bits. Input and output interfaces are based on MTJs
b Racetrack logic. Two magnets are placed around magnetic wire, their magnetic field is used to locally change logic values stored inside memory

Background: Racetrack memory was initially proposed in [1] as an high-density non-volatile memory. A racetrack memory uses a ferromagnetic nanowire to embed information encoded as digital values. Every nanowire can memorise several bits. The first prototype of a racetrack memory integrated with a CMOS circuit was presented in [3], using a 90 nm technological process. Racetrack memories can be fabricated using both in-plane magnetisation materials [1] and out-of-plane magnetisation materials [4]. The use of out-of-plane magnetisation allows to build high-density low power consumption memories [4]. The cost is an increment of the complexity in the fabrication process of the ferromagnetic materials employed. Recently, racetrack memories were also used as building block for non-volatile CMOS hybrid logic circuits [5].

Proposed architecture: The basic structure of a racetrack memory is depicted in Fig. 1*a*. A long ferromagnetic wire is used to store a large amount of logic values. Notches are created along the magnetic stripe to physically separate one bit from the other. Each section of the memory can be only in one of two stable states, used therefore to represent digital values. To write inside the memory two techniques can be employed. A magnetic field, locally applied to one section of the memory, can be used to write a new bit inside the memory. Another possibility is to build a magneto-tunnel junction (MTJ) on top of the magnetic wire. When a current flows through the MTJ the magnetisation of the stripe is altered locally, writing a new bit inside the memory. Similarly, MTJs can be used as output sensors, given that their resistance change accordingly to their magnetic state. If a current flows through the magnetic wire the information stored can be shifted forward or backward, depending on the direction of the current. A racetrack memory, with the structure depicted in Fig. 1*a*, can be therefore assimilated to a first-in-first-out serial memory.

The physical structure of the racetrack logic element that we propose is instead highlighted in Fig. 1*b*. Two magnets are placed around the central section of the magnetic strip. These magnets can be either fixed value magnets or MTJs, for a full programmable logic. Aside from these additional magnets the structure remains the same as a normal racetrack memory.

The working principle of the racetrack logic here proposed is explained in Fig. 2. The basic idea is to exploit the same mechanism that can be used to write the memory. A local magnetic field is able to switch one bit of the memory to one stable state to the other. Instead of generating that magnetic field using, for example, a current flowing through a wire, we use additional magnets placed around one section of the magnetic strip. As depicted in Fig. 2*a*, the section of the memory surrounded by the two magnets is subjected to four magnetic fields. These magnetic fields are the magnetic fields generated by the two additional magnets and the magnetic fields generated by the two neighbour sections of the memory. Normally the sum of these magnetic fields is not enough to cause a local switch of the magnetisation. If an external magnetic field is added (Fig. 2*b*), the sum of this magnetic field and the magnetic fields generated by the magnets is enough to overcome the critical magnetic field, causing a local flip of the magnetisation. The magnetisation is therefore switched from one stable state to the other directly, without the need to force the magnetic line in an intermediate unstable state. Furthermore, the switch depends on the state of neighbour elements, so it is a logic combination of their values. It is a true logic-in-memory operation. The magnetic field is a bidirectional global magnetic field applied to the whole chip. If it is not applied the circuit behaves exactly as a memory. When the magnetic field is applied, the values stored inside the memory can be altered according to a logic combination of all inputs. Further details on the logic behaviour of the circuit will be given in the section describing the equivalent circuit.

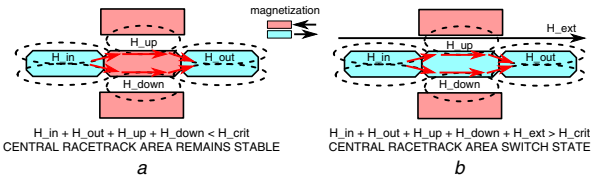

Fig. 2 *Racetrack logic working principle*

a Central element of racetrack wire is influenced by magnetic field generated by both additional magnets and neighbour parts of magnetic stripe. Sum of these magnetic fields is not enough to cause a switch in magnetisation of strip
b If external magnetic field is applied to whole circuit, then sum of all magnetic fields is enough to generate local switch of magnetisation

Simulation results: To validate this idea we performed a detailed characterisation of the proposed structure using micromagnetic simulations. The simulator that we used is Mumax3 [6], a GPU-accelerated physical simulator. The use of Mumax3 allowed us to use a very fine mesh ($2 \times 2 \times 2$ nm^3) and to include the effect of thermal noise, obtaining therefore a very accurate simulation of the structure. The magnetic memory strip is made by several sections. Each section has a length of 120 nm and an height of 40 nm. The two additional magnets are 120 nm long and have an height of 40 nm. They are separated by a distance of 10 nm from the memory. The thickness of all the magnetic structures is 6 nm. The material used is Permalloy, which has an in-plane magnetisation. Most of the research on racetrack memories is focused on out-of-plane magnetisation materials, because they offer better performance and more reliability. In this case, we wanted to demonstrate the validity of our idea, not to optimise the structure for the best performance. We choose therefore to use Permalloy as material because it is a widely known material and easy to model. This choice therefore strengthens the validity of the results that we obtain.

Fig. 3 depicts an example of physical simulation obtained. In the initial state (Fig. 3*a*), the magnetisation of all magnetic elements, except one, is aligned along the longer side of the magnets pointing leftward. The element of the magnetic memory on the left of the central area is

instead forced in the opposite state, with magnetisation pointing rightward. Then a global magnetic field of 16 kA/m is applied to the structure. The magnetic field is also applied along the x-axis, therefore parallel to the longer magnets side. The applied magnetic field points rightward, so it is parallel to the magnetic field generated by the two additional magnets and the magnetic field generated by the left element of the memory. As highlighted in Fig. 3*b*, the central element correctly switch from one state to its opposite. Of course to validate the structure one simulation is not sufficient. We tested the structure in all 64 possible combinations of state and we verified that effectively the structure behaves as intended. For example, if we invert the state of the two additional magnets there is no switch. We cannot present additional simulations in different conditions or report the complete table of truth of the logic element due to the limited space available. In the next section, we report the logic function of the racetrack logic and a detailed description of its behaviour. The switching time is smaller than 1 ns. Considering that the value of applied magnetic field is also very small, we can conclude that the circuit has also excellent performance.

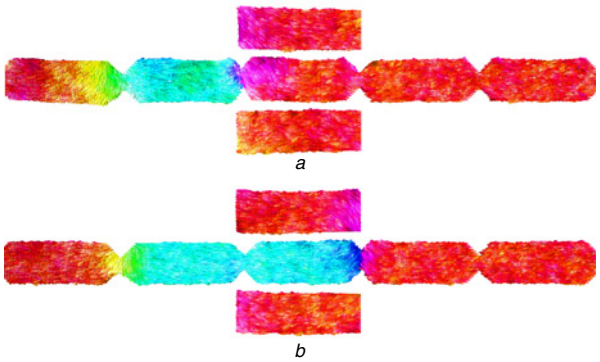

Fig. 3 *Physical simulation of a racetrack logic element*

a Initial state, magnetisation of all elements is parallel to longer magnets side, pointing leftward. Only element of racetrack memory on left of central area is forced in opposite direction, with magnetisation pointing rightward
b When a global magnetic field pointing rightward is applied to structure, magnetisation of central element of memory switches to opposite state

Equivalent circuit: Fig. 4 depicts the complete equivalent circuit of the racetrack logic. Considering the memory part alone, its equivalent circuit can be represented as a bidirectional shift register. Every part of the magnetic wire is modelled by a latch, where the clock is the current flowing through the wire itself. The direction of the applied current controls the input multiplexer, deciding therefore the direction of the shift. The behaviour of the logic part of the circuit can be summarised by the equation

$$\mathrm{EVAL} = \mathrm{MV}(\mathrm{MAG.FIELD}, \mathrm{INPUT}, \mathrm{OUTPUT}, \overline{\mathrm{UP}}, \overline{\mathrm{DOWN}}).$$

It is a 5-input majority voter, where the output (EVAL) is the value of the central part of the memory wire. The inputs are the external magnetic field, the inverted values of the up (UP) and down (DOWN) magnets and the values of the neighbour areas of the memory wire, INPUT and OUTPUT (see Fig. 1*b*). In addition to this behaviour, the value of EVAL can switch only if the applied magnetic field is in the opposite state to it. This peculiarity is modelled by the exor gate in Fig. 4.

If we suppose to control independently all the inputs of the logic gate, by setting, for example, MTJs on both the additional magnets and the left and right parts of the central memory element, we obtain exactly a combinational gate. It is a powerful logic gate with a relative small circuit area. Considering instead the circuit as it will be used, where the input and the output interface of the memory are generally placed on the extremities of the wire, then the behaviour became more complex. The logic behaves still as a 5-input majority voter, but, by shifting the information using the current, the values of INPUT and OUTPUT depend on the previous state of the circuit. The behaviour is no more combinational but sequential, and the whole circuits behave like a very compact finite-state machine. This peculiar behaviour can open up interesting new ways of designing logic circuits.

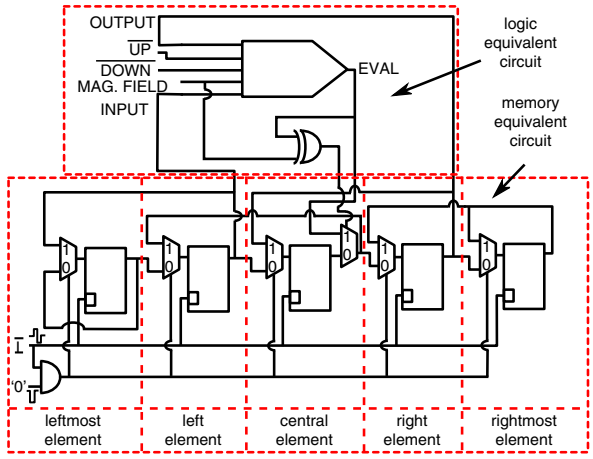

Fig. 4 *Racetrack logic equivalent circuit. Memory part is equivalent to a shift register, where every register represents one element of magnetic wire. Current is clock of registers, while its direction decides shift verse. Logic part is equivalent to a 5-input majority voter, where inputs are inverted values of two additional magnets, value of neighbour memory elements and external magnetic field. Value of central memory element can change only if applied magnetic field is in opposite direction (exor gate)*

Conclusion: We have proposed an innovative approach to use a racetrack memory not only as a memory, but also to perform in-memory logic computations. The racetrack logic concept is based on the simple addition of two magnets and a global magnetic field, performing a bitwise majority logic on the information stored in the memory. The obtained circuit is a 5-input majority voter, a powerful and compact logic gate. Furthermore, considering that a racetrack memory is equivalent to a shift register, the proposed circuits behave like a compact finite-state machine.

Now that we have demonstrated the feasibility of this idea, we are focusing on solving the critical issues identified by our first analysis. First, we will improve the magnetic coupling with the additional magnets, by placing them on top and on bottom of the memory wire, reducing at the same time the distances. Second, we will investigate how to improve the reliability and the performance of the circuit by using perpendicular magnetic anisotropy materials.

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One or more of the Figures in this Letter are available in colour online.

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