nature COMMUNICATIONS

ARTICLE

Received 13 Dec 2016 | Accepted 11 May 2017 | Published 26 Jun 2017

DOI: 10.1038/ncomms15891 OPEN

Rewritable ghost floating gates by tunnelling triboelectrification for two-dimensional electronics

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Gates can electrostatically control charges inside two-dimensional materials. However, integrating independent gates typically requires depositing and patterning suitable insulators and conductors. Moreover, after manufacturing, gates are unchangeable. Here we introduce tunnelling triboelectrification for localizing electric charges in very close proximity of two-dimensional materials. As representative materials, we use chemical vapour deposition graphene deposited on a SiO_2/Si substrate. The triboelectric charges, generated by friction with a Pt-coated atomic force microscope tip and injected through defects, are trapped at the air–SiO_2 interface underneath graphene and act as ghost floating gates. Tunnelling triboelectrification uniquely permits to create, modify and destroy p and n regions at will with the spatial resolution of atomic force microscopes. As a proof of concept, we draw rewritable p/n^+ and p/p^+ junctions with resolutions as small as 200 nm. Our results open the way to time-variant two-dimensional electronics where conductors, p and n regions can be defined on demand.

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In conventional field-effect devices[1,2], the gate voltage electrostatically controls charge carriers inside a semiconductive channel, which is separated from the gate by an insulating layer. This gate-driven electrostatic control of charge carriers has been demonstrated for graphene[3,4] and other two-dimensional (2D) materials[5,6]. Moreover, it is relatively easy to integrate on a single chip many 2D field-effect devices sharing a single global bottom gate. However, the very large-scale integration (VLSI) of independent field-effect devices on a single chip is very complex. In fact, similar to state-of-the-art complementary metal-oxide semiconductor (CMOS) devices, the fabrication of independent gates, insulating layers and channels requires the growth and patterning of different, high-quality and carefully selected materials[7,8], with intricate process-compatibility issues. This problem is exacerbated by severe geometrical constraints; in fact, besides the quest for ultra-small gate dimensions, the insulating layer must be extremely thin to guarantee an effective (that is, with reasonably low voltages) electrostatic induction of charges in the channel. In addition, in conventional electronics, once the circuit has been manufactured, its structure and, in particular, the positions and shapes of all the gates may not be modified.

Triboelectrification is the electrical charging by friction between two materials[9–11]. Although the triboelectric effect is reported to have been first observed by Thales of Miletus, it is still a subject of intense research and, recently, has been investigated, with nanoscale spatial resolution, by using atomic force microscopy (AFM). In practice, by rubbing insulators with the tips of AFM[12,13], electrical charges can be localized on insulators and be stored for relatively long periods, around 1 h.

Here we introduce tunnelling triboelectrification for defining on-demand rewritable ghost floating gates below a 2D material with the spatial resolution of AFMs[14,15]. Tunnelling triboelectrification is the friction-induced tunnelling of charges through a 2D material and their accurate localization on the insulator underneath the 2D material. Tunnelling of charges may also occur in conventional triboelectrification processes, but in tunnelling triboelectrification charges tunnel through a 2D material rather than simply through air or vacuum. Moreover, though charges can be localized even by conventional triboelectrification of dielectrics such as SiO_2 (refs 12,13), the charges injected by tunnelling triboelectrification exhibit impressively longer lifetimes (for example, more than two order of magnitude longer). Finally, after tunnelling triboelectrification, the charges very effectively control the properties of the 2D material, thus behaving as immaterial, charges-only, ghost floating gates, which can be repeatedly created, modified or destroyed; this unique property may be the key for the development of novel 2D devices, which can be drawn or modified on demand.

Results

Tunnelling triboelectrification. We deposited CVD graphene on a SiO_2 (300 nm)/Si wafer using a wet transfer method. As schematically shown in Fig. 1a, with silicon connected to ground, we rubbed the CVD graphene over a $0.5 \times 0.5\,\mu m^2$ area using a grounded Pt-coated AFM tip in contact mode, with a force of 15 nN. We verified by AFM that rubbing does not result in detectable mechanical damages to graphene (Supplementary Note 1 and Supplementary Fig. 1) and also measured the thickness of the unavoidable air-gap between graphene and SiO_2 substrate, which is around 0.66 nm[16,17] (Supplementary Fig. 2). To measure the surface potential, both before and after triboelectrification[18,19], we have used Kelvin probe force microscopy (KPFM)[20,21]. Figure 1b shows the initial state of the CVD graphene surface potential on a $1.5 \times 1.5\,\mu m^2$ area; as evident, before rubbing, graphene is equipotential, except random fluctuations (for example, due to undesired trapped charges and contamination). Figure 1c shows the surface potential in the entire $1.5 \times 1.5\,\mu m^2$ area after rubbing the $0.5 \times 0.5\,\mu m^2$ central square; the rubbed region has a $\sim$50 mV higher surface potential than the unrubbed region. Such potential variation may not be attributed to charges stored in the graphene as electric charges may be localized for long times only in insulating materials. We therefore conclude that some of the charges generated during rubbing tunnel through the monolayer graphene and are locally trapped on the underlying insulator. The trapped charges act as an immaterial (that is, made of charges-only and not of a conductor), bottom floating gate and locally change the polarity and density of charges in graphene as well as the graphene work-function; for simplicity we will therefore refer to these trapped charges as to ghost floating gates. The ghost floating gates effectively control the carriers within graphene because of the ultimate thinness of graphene as well as of the comparably thin air-gap.

Figure 1d shows the averaged ΔV_{TT} (across the central 0.5 μm horizontal stripe; the average is computed to reduce the effect of random fluctuations) as a function of position (along the black dashed line of Fig. 1c) taken immediately after rubbing and after 72 h (Supplementary Fig. 4 shows the original KPFM maps), where, to highlight the effects of rubbing rather than random fluctuations, ΔV_{TT} is defined as the surface potential taken with reference to the average surface potential of the unrubbed region (that is, ΔV_{TT} shows the net variations of the surface potential, due to tunnelling triboelectrification, in the rubbed region in comparison with the unrubbed region). As evident, the potential variation is very well preserved even after 72 h. Figure 1e shows the averaged ΔV_{TT} as a function of time and the best fit function (blue line)

$$\Delta V_{TT}(t) \simeq 4\mathrm{mV} * e^{\frac{-t}{\tau_{short}}} + 46\mathrm{mV} * e^{\frac{-t}{\tau_{long}}}. \quad (1)$$

In practice, along with a small term, which has a shorter time constant ($\tau_{short} \sim 3$ h and 21 min), there is a dominant term with much higher initial amplitude and with an exceptionally long time constant ($\tau_{long} \sim 278$ h, that is, more than two orders of magnitude higher than the decay time, around 1 h[13], of conventional triboelectrification on a SiO_2 dielectric with the same thickness, 300 nm, as in our experiments, Supplementary Note 3.3 and Supplementary Fig. 10). The Supplementary Note 2 and Supplementary Figs 3–6, 13 show additional experiments which further confirm the proposed tunnelling triboelectrification mechanism.

To gain further insight on tunnelling triboelectrification, we also studied the cases of monolayer (1L), bilayer (2L), trilayer (3L) CVD graphene and highly ordered pyrolytic graphite (HOPG). Similar to the experiments described in Fig. 1, we used SiO_2 (300 nm)/Si substrates, and measured the surface potential of a $2 \times 2\,\mu m^2$ graphene layer both before and after rubbing the $1 \times 1\,\mu m^2$ central area with a Pt AFM tip. Figure 2a shows, for each sample, the average surface potential changes which result from rubbing ($\Delta V_{after-before}$), both in the rubbed (ΔV_r) and in the unrubbed (ΔV_u) parts of the graphene films. ΔV_r (red line in Fig. 2a) decreases as the number of graphene layers increases; by contrast, ΔV_u (black line in Fig. 2a) increases and, for highly ordered pyrolytic graphite (HOPG), both ΔV_r and ΔV_u converge to the same value, similar to what would happen without tunnelling triboelectrification, that is, the film would be equipotential (except random fluctuations) and the triboelectric charges would simply charge the graphene–air–SiO_2–silicon capacitor. Except for HOPG, the graphene layers are not equipotential as the trapped charges, similar to the presence of ghost floating gates at the SiO_2–air interface, locally increase or decrease, depending on their polarities, the graphene potential. In practice, tunnelling triboelectrification and the spread of charges on the entire graphene layer are two competing processes.

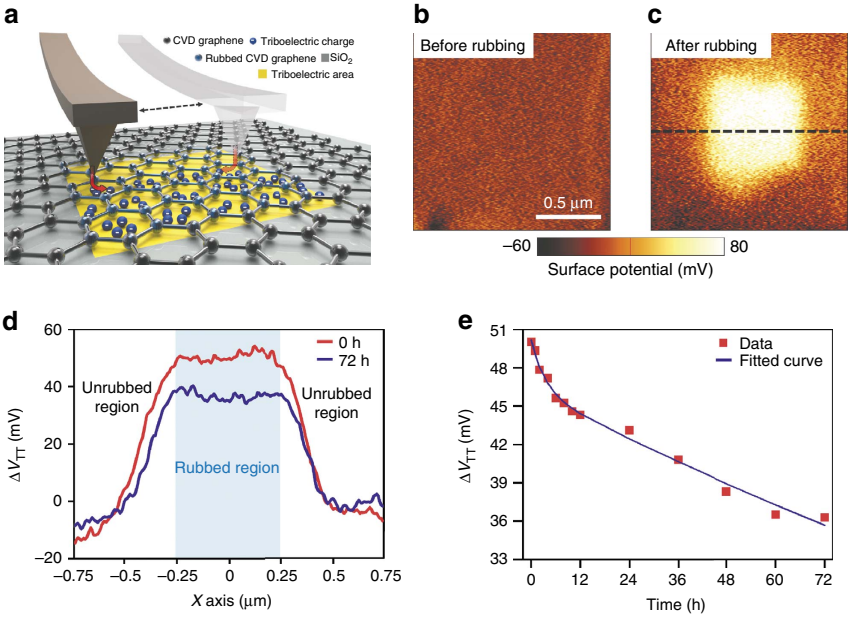

Figure 1 | Tunnelling triboelectrification by friction of graphene with a Pt AFM tip. (**a**) Schematic of the friction process and the KPFM measurement system. (**b**) KPFM image of graphene before rubbing. (**c**) KPFM image of graphene after rubbing. (**d**) Potential difference generated by tunnelling triboelectrification, ΔV_{TT}, along the blue dashed line in **c** after 0 and 72 h; ΔV_{TT} is very well preserved even after 72 h. (**e**) ΔV_{TT} as a function of time and best fit (blue line) with the sum of two decaying exponential terms, each with its own time constant.

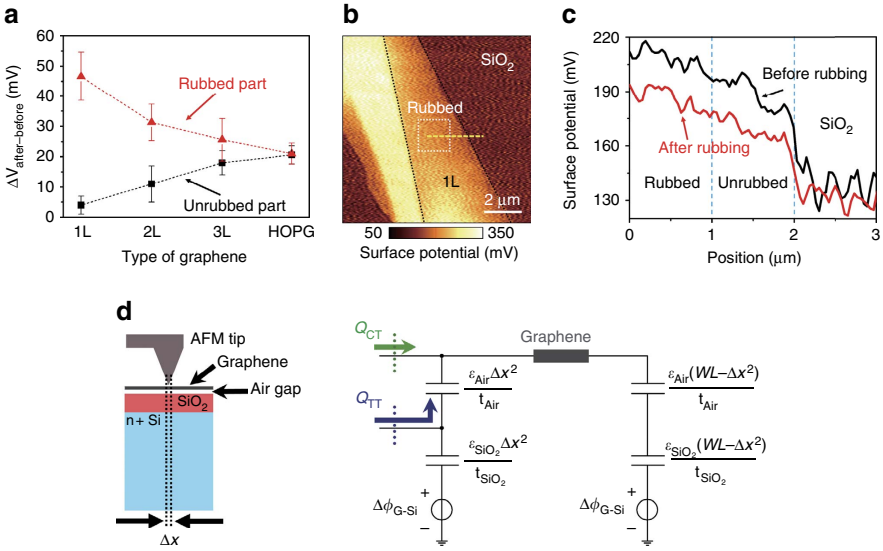

Figure 2 | Tunnelling triboelectrification with different types of graphene and equivalent circuit. (**a**) ΔV_r and ΔV_u for different types of CVD graphene (1, 2 or 3 layers) and for HOPG. (**b**) KPFM image of mechanically exfoliated graphene (MEG) after rubbing with an AFM tip. (**c**) KPFM image of the MEG layer measured along the yellow dashed line in **b** and showing that there is no significant potential difference between the rubbed and unrubbed parts (the almost constant shift is due to triboelectric charges spreading all over the graphene layer and thus charging the graphene-to-silicon capacitor). (**d**) Schematic diagram (not to scale) and simplified, lumped elements equivalent circuit for the tunnelling triboelectrification process; the equivalent circuit comprises the small areas (Δx^2) air-gap and SiO_2 capacitors (rubbed section) and the large area capacitors (rest of the graphene layer). Error bars are defined as s.e.m.

The spread of charges involves the entire graphene layer and is global; on the contrary, tunnelling triboelectrification is restricted to an area of graphene comparable with the contact area of the AFM tip and, therefore, is extremely localized. As evident from Fig. 2a, for 1L CVD graphene the tunnelling triboelectrification charges are almost identical to the entire triboelectric charges; in fact, for monolayer CVD graphene, tunnelling triboelectrification prevails over the spread of charges on the entire graphene layer because of the ultimate thinness of graphene as well as of the extremely high speed of tunnelling processes, which take much less time than charging the graphene–air–SiO_2–silicon capacitor. By contrast, when increasing the number of layers, tunnelling becomes more and more unlikely and triboelectric charges tend to spread over the entire graphene layer and, consequently, increase or decrease the potential of the entire graphene layer.

We also performed similar experiments on mechanically exfoliated graphene on SiO_2/Si substrates. Figure 2b shows the surface potential of monolayer exfoliated graphene (MEG)

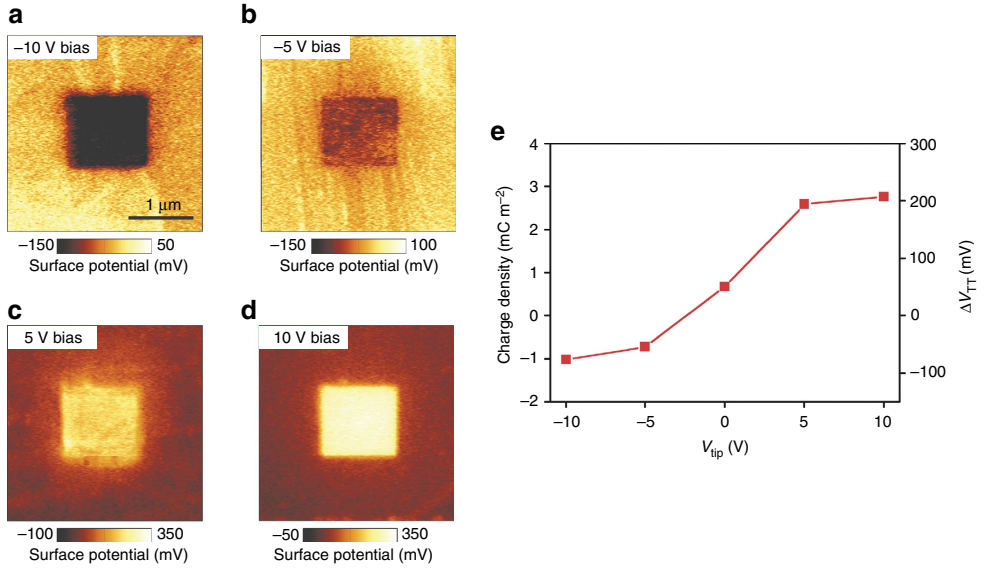

Figure 3 | Control of the density and polarity of the tunnelling triboelectric charges. (**a**–**d**) KPFM images of graphene after rubbing the central area with different tip bias voltages of (**a**) −10 V, (**b**) −5 V, (**c**) 5 V, (**d**) 10 V. (**e**) Triboelectric charge density and potential drop induced by tunnelling triboelectrification (ΔV_{TT}) as a function of the tip bias. The polarity and amount of the tunnelling triboelectric charges can be controlled by the tip bias voltage.

(black dashed line region) after rubbing an area of $1.5 \times 1.5\,\mu m^2$ (white box region) with the Pt AFM tip. As shown in Fig. 2c, contrary to CVD graphene, triboelectric charges do not tunnel and, except random fluctuations, there is no detectable potential difference between the rubbed and unrubbed areas. Instead, the surface potential of the entire MEG region, both rubbed and unrubbed parts, changes by a constant quantity, similar to the case of HOPG. These results further confirm the proposed mechanism because defect regions such as grain boundaries have higher empty state tunnelling transmission coefficients than bulk graphene[22,23], so that charges generated by rubbing can more easily pass through the defective 1L CVD graphene. By contrast, MEG, though monolayer, has less defects (Supplementary Fig. 7) and, therefore, the triboelectric charges diffuse along the whole MEG layer. In conclusion, the triboelectric charge localization is most effective in 1L CVD graphene due to both its single-atomic thickness and high-defect density.

Figure 2d schematically illustrates that the tunnelling triboelectrification process is confined in an extremely small area with a characteristic length Δx comparable with the very sharp tip of the AFM. In the simplified, lumped elements, equivalent circuit for tunnelling triboelectrification shown in Fig. 2d, we distinguish the small area, rubbed section (capacitors with area Δx^2) and the global section (capacitors relative to the rest of the graphene layer, with area approximately equal to the entire graphene area, WL). Owing to rubbing, a fraction of the triboelectric charges tunnel through graphene and is injected at the interface between air and SiO_2 (tunnelling triboelectric charges, Q_{TT}); the rest of the triboelectric charges (complementary-triboelectrification charges, Q_{CT}) spreads all over the graphene layer. Immediately after tunnelling, the charges Q_{TT}, trapped at the air–SiO_2 interface, electrostatically attract charges of the opposite type on the graphene layer and/or on the silicon underneath silicon oxide (that is, the charges Q_{TT} may not travel through dielectrics and therefore must be stored on the top plate of the SiO_2 small-area capacitor and/or on the bottom plate of the small-area air capacitor). However, as graphically illustrated in Fig. 2d, almost all these opposite charges are attracted from graphene because of the much smaller thickness (that is, larger capacitance) of the small-area air capacitor in comparison with the small-area SiO_2 capacitor (Supplementary Note 3 and Supplementary Figs 8–10). With reference to the equivalent circuit, the charges Q_{TT} are almost all stored on the bottom plate of the small-area air capacitor and then act as a ghost floating gate which is not manufactured but can be triboelectrically drawn and deleted at will by the AFM tip. Since almost no charges go towards the small-area SiO_2 capacitor, its voltage is almost unaffected and, therefore, the voltage drop across the small-area air capacitor is almost exactly the same as the voltage drop measured across graphene by KPFM, that is, ΔV_{TT}. Remarkably, since the air-gap is extremely thin (about 0.66 nm, that is, comparable with the equivalent oxide thicknesses of state of the art CMOS devices, Supplementary Fig. 2), the charges Q_{TT} very effectively control the current transport inside graphene. Moreover, despite the very small air-gap thickness, the ghost floating gate does not introduce significant parasitic capacitance as, dynamically, the series of the oxide and air capacitance is almost identical to the silicon oxide capacitance alone. The equivalent circuit shown in Fig. 2d also gives reasons for the exceptionally long decay time of tunnelling triboelectrification charges (Fig. 1e). In fact, since, after triboelectrification, there is no current flow through graphene (the potential drop across graphene may not result in a net current flow because of the competing electrostatic attraction from the charges stored on the immaterial ghost gate), both the air-gap and the SiO_2 capacitors can only be discharged by their leakage currents (Supplementary Note 3.3), thus resulting in two time constants associated to the air-gap and the SiO_2 capacitors, respectively. In conclusion, first, in regions subject to tunnelling triboelectrification, the air-gap capacitors are charged to comparatively much higher voltages than SiO_2 capacitors because the tunnelling triboelectric charges almost entirely go towards the bottom plates of air-gap capacitors. Second, the total voltage is the sum of two terms, each with its own time constant; the dominant term, relative to the air-gap capacitor, has a much larger time constant because air is a much better insulator than SiO_2, in perfect agreement with our experimental results (two time constants best fit in Fig. 1e). The excellent insulation properties of air also justify the exceptionally long decay of the tunnelling triboelectrification voltages in comparison with conventional triboelectrification[12,13].

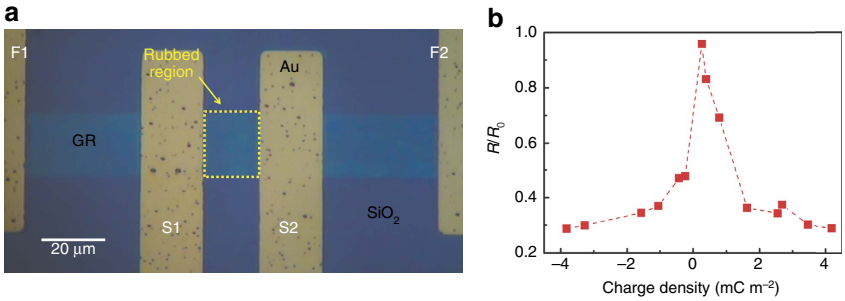

Figure 4 | Resistance reduction of graphene by tunnelling triboelectrification. (**a**) Optical image of the 4-wires graphene resistor (the yellow dashed box is rubbed by the Pt AFM tip). (**b**) Normalized resistance R/R_0 of the graphene resistor as a function of the tunnelling triboelectric charge density.

In conventional triboelectrification, both the density and polarity (positive or negative) of the triboelectric charges injected into a rubbed insulating material can be controlled by the application of a biasing voltage V_{tip} to the Pt AFM tip during rubbing[13]. Therefore, since the tunnelling triboelectrification charges Q_{TT} are a fraction of the total triboelectric charges, both the density and polarity of the trapped charges as well as the sign of the voltage drop between the rubbed and the unrubbed parts of graphene can be controlled by changing the tip biasing voltage. Consistently, Fig. 3a–d show ΔV_{TT} after the central square has been rubbed with the Pt AFM tip biased at voltages ranging from -10 to $+10$ V. At negative biasing voltages (Fig. 3a,b), negative charges are trapped and attract holes in the rubbed part of the graphene, thus increasing the natural p-type conductivity of CVD graphene. On the contrary, at positive biasing voltages (Fig. 3c,d), positive charges are injected and attract electrons in the rubbed part of the graphene so that, at sufficiently high biasing voltages, graphene is inverted to n-type conductivity. Figure 3e shows the average surface potential of the rubbed part, taken with reference to the unrubbed part, as a function of V_{tip}. Since the surface potential, taken with reference to the potential of the unrubbed part, is almost identical to the voltage locally stored across the small-area air-gap capacitors, the tunnelling triboelectric charges surface density (Fig. 3e) can be computed as the voltage drop across the air-gap capacitor multiplied by the air-gap capacitance per unit area $\varepsilon_{Air}/t_{Air}$, where ε_{Air} is the dielectric constant of air and t_{Air} is the thickness of the air-gap.

Tunnelling triboelectrification also allows to control the resistivity of graphene. As an example, we fabricated the 4-contacts 1L CVD graphene resistor shown in Fig. 4a. The middle area of the graphene resistor (yellow dashed box, $17 \times 20\,\mu m^2$, between the sense electrodes S1 and S2 in Fig. 4a) was rubbed by a Pt tip. The voltage difference of the 1L CVD graphene between the inner electrodes S1 and S2 was measured in vacuum by applying a constant current through the external force electrodes F1 and F2. During the measurements, we kept the current at a very low level (that is, 100 nA) to prevent any perturbation of the stored charges. In fact, the tunnelling triboelectric charges stored underneath graphene may be removed at sufficiently high currents. Although the threshold current depends on the sample, we found that trapped charges may survive even under currents up to the mA range for widths of only 20 μm (Supplementary Fig. 11). Figure 4b shows the normalized resistance R/R_0 (where R is the resistance of graphene after rubbing and R_0 is the resistance before rubbing) as a function of the tunnelling triboelectric charge density (See Supplementary Note 4.1 and Supplementary Fig. 12 for details). As expected, the tunnelling triboelectric charges act as ghost floating gates and electrostatically reduce the resistivity (for example, up to three times at room temperature with magnitude of the biasing tip voltage limited to 10 V). The dependence of the resistance on the tip voltage is obviously similar to the gate bias-dependent resistance in graphene field-effect devices[3,24] with conventional gates. Moreover, we also verified that tunnelling triboelectrification allows to control the Dirac point of graphene in practical graphene field effect devices (Supplementary Note 4.2 and Supplementary Fig. 13).

Rewritable floating gates. Tunnelling triboelectrification allows the local and dynamic control of both the polarity and the density of free carriers in 2D materials with the extraordinary spatial resolution of AFMs. In particular, the dimensions and shapes of ghost floating gates or, equivalently, of p and n regions as well as of conductors (for example, made of very highly doped regions) can be dynamically changed over time, possibly resulting in truly time-variant electronic devices and systems. Since AFMs can be fully integrated on a single chip[25–27], we envision single chips comprising the AFM and regions of 2D materials whose properties can be controlled on demand by tunnelling triboelectrification. This approach would be similar to the memory refresh process (that is, periodically reading and immediately rewriting the same information on capacitive memories to counteract the degradation of information due to leakage currents) routinely used in dynamic random-access memories (DRAM). We also observe that tunnelling triboelectrification would also allow to simultaneously take advantage of different 2D materials on a single substrate without the intricacies of co-integrating suitable gates and insulating layers for different 2D materials (to manufacture conventional gates, each 2D material would require its own processing, including patterning of carefully selected materials as both insulators and gates). As a proof of concept, Fig. 5 shows several time-variant p/p^+ (Fig. 5a) and p/n^+ (Fig. 5b) junctions with resolutions as small as 200 nm. These p/p^+ and p/n^+ junctions are associated to rewritable ghost floating gates that can be repeatedly created, modified and erased. This is the first report of gates, p/p^+ and p/n^+ junctions whose shapes and charges can be defined on demand with deep sub-micron resolution.

Discussion

In conclusion, we have introduced tunnelling triboelectrification for dynamically localizing charges on immaterial, floating, bottom ghost gates underneath 2D materials. We rubbed graphene with a Pt-coated AFM tip and found that a fraction of the triboelectric charges, generated by friction between graphene and the AFM tip, tunnel through graphene and are trapped at the interface between the air-gap and the underlying insulator (SiO_2, mica or Al_2O_3 in our experiments). Tunnelling triboelectrification occurs in defective CVD graphene, especially for single-layer samples, but not in high-quality exfoliated graphene or in HOPG. We also

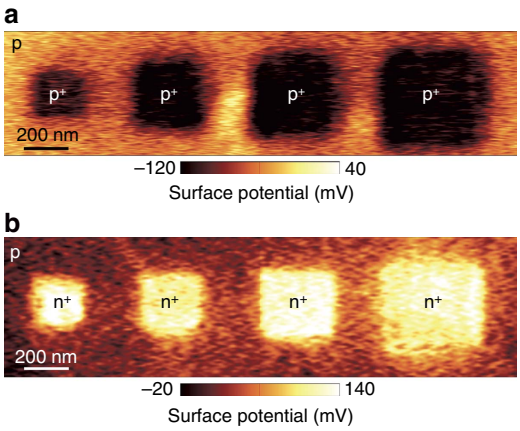

Figure 5 | Rewritable p/p$^+$ and p/n$^+$ junctions and ghost floating gates. (**a**) KPFM image of four deep sub-micron p/p$^+$ junctions defined by selectively rubbing arbitrary square graphene regions with the AFM tip biased by −10 V; each p/p$^+$ junction corresponds to an underlying ghost rewritable floating gate. The sides of each rubbed region are 200, 300, 400 and 500 nm, respectively, from left to right. (**b**) KPFM image of four deep sub-micron p/n$^+$ junctions defined by selectively rubbing arbitrary square graphene regions with the AFM tip biased by 10 V. The sides of each rubbed region are 200, 300, 400 and 500 nm, respectively, from left to right.

found a decay time of several days, which is more than two orders of magnitude longer than for standard triboelectrification. Owing to the ultimate thinness of 2D materials and to the sub-nanometer insulating air-gap, the immaterial ghost gates very effectively control charges inside graphene. In striking contrast with conventional electronic devices which, after manufacturing, may not be changed, the ghost floating gates as well as the resulting p and n regions can be created, enlarged, reduced or destroyed on-demand, with the resolution of AFMs and without the intricate process-compatibility issues for integrating many independent conventional field-effect devices on a single chip. Although these immaterial ghost gates are floating, with obvious restrictions for the design of analogue and digital circuits[28–32], other types of devices and transistors (for example, bipolar junction transistors) can also be fabricated by taking advantage of ghost floating gates. We also mention that tunnelling triboelectrification may easily be combined with conventional microfabrication technologies; for instance, in our experiments, we have deposited graphene on a conventional SiO_2/Si substrate, which is obviously compatible with the integration of CMOS analogue/digital circuits and/or MEMS, including micromachined AFMs. In fact, since AFMs can be fully integrated on a single chip[25–27], in contrast with conventional 'time invariant' micro devices whose gates, p and n regions are unchangeable, we envision systems-on-chip[33–39] or systems-in-package[40], where ghost floating gates and n and p regions are continuously, on-demand defined, modified or destroyed by tunnelling triboelectrification. As a proof of concept, we have dynamically defined several p/n$^+$ and p/p$^+$ junctions with resolutions as small as 200 nm. Our results may greatly facilitate the very large-scale integration of independent 2D field-effect devices and can open the way to time-variant 2D electronics, where conductors (for example, very highly doped regions), p and n regions can be defined on demand.

Methods

Synthesis of CVD graphene and transfer method. A 75 μm-thick copper foil (Wacopa) was used for graphene growth. The copper foil was placed in a rapid thermal chemical vapour deposition (CVD) chamber, where the temperature was increased from room temperature to 1,000 °C under a 10 sccm flow of H_2 (1 Torr). Then, the copper foil was annealed for 30 min to clean its surface. The CVD graphene was synthesized by a mixture of CH_4 (20 sccm) and H_2 (10 sccm) for 30 min (1 Torr). After the growth was complete, the gas supply was ceased and the chamber was cooled below 100 °C at a cooling rate of 160 °C min^{-1}. The CVD graphene synthesized on copper foil was spin-coated with poly(methyl methacrylate) (PMMA) using spin coater with 1,000 r.p.m., 30 s and it was cured at 120 °C for 10 min. Then, the CVD graphene on copper foil was floated in an etchant (Transene, type 1) to etch away the copper foil. After the copper foil was completely etched away, the graphene with PMMA was rinsed in deionized water three times to wash away the etchant residues. The CVD graphene was transferred onto SiO_2 (300 nm)/Si (boron doped p-type, resistivity is 70 Ohm cm) substrate using a well-known wet transfer method. Multi-layer CVD graphene was prepared by repeating the same process[11].

Generation and measurement of triboelectric charges. The rubbing process between a Pt-coated tip (Multi75E-G, Budget Sensors) and graphene was carried out by the contact mode of an AFM system (XE100, Park Systems) under a contact force of 15 nN and at a scan rate of 1 Hz, to generate triboelectric charges. In the experiments of Figs 3 and 4, we applied a tip bias from −10 to 10 V on each sample with the conditions otherwise the same. The Kelvin probe force microscopy (KPFM) maps have been obtained with the tip biased by an AC voltage having amplitude and frequency equal to 2 V and 17 kHz, respectively. In addition, all AFM-based measurements progressed under the same conditions (temperature = 21 °C, relative humidity = 25 ~ 30%).

Data availability. The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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Acknowledgements

This project was financially supported by the Basic Science Research Program (2015R1A2A1A05001851) through the National Research Foundation (NRF) of Korea Grant funded by the Ministry of Science, ICT & Future Planning. SKKU has filed a patent related to this work.

Author contributions

S.K., T.Y.K., S.-W.K and C.F. designed and conceptualized the project. S.K., T.Y.K., K.H.L., S.-W.K. and C.F. designed the experiments. K.H.L. and T.-H.K. synthesized graphene samples in the CVD process and fabricated devices. T.Y.K., R.H. and F.A.C. performed simulations. S.K., T.Y.K., S.K.K. and R.H. conducted the AFM and KPFM experiments and characterization. S.K., T.Y.K., K.H.L., R.H. and F.A.C. analysed the data. C.F. and S.-W.K. supervised the overall conception and design of this project. All authors contributed to the writing of the paper.

Additional information

Supplementary Information accompanies this paper at http://www.nature.com/naturecommunications

Competing interests: S.K., T.Y.K, K.H.L, S.K.K, C.F. and S.-W.K are co-inventors of the patent entitled 'Method for controlling electrical property of 2D material using triboelectrification' patent number: 10-1557246, South Korea. The remaining authors declare no competing financial interests.

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How to cite this article: Kim, S. *et al.* Rewritable ghost floating gates by tunnelling triboelectrification for two-dimensional electronics. *Nat. Commun.* **8**, 15891 doi: 10.1038/ncomms15891 (2017).

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File name: Supplementary Information

Description: Supplementary Figures, Supplementary Notes and Supplementary References

Supplementary Note 1. Mechanical stability of graphene after rubbing

The generation of triboelectric charges involves mechanical friction between the Pt-coated atomic force microscope (AFM) tip and graphene. In order to exclude damages to graphene, we analyzed topographic images of chemical vapor deposition (CVD) graphene after the rubbing process; Supplementary Fig. 1a shows a representative measurement. The white dashed box indicates the rubbed region. As evident, there is no detectable difference between the rubbed and unrubbed regions, consistently with the good mechanical durability of graphene[1, 2]. In addition, the cross section profile of Supplementary Fig. 1a along the blue dashed line shows no height difference between the two regions (Supplementary Fig. 1b). We conclude that our rubbing procedure does not result in significant damages for graphene.

Supplementary Note 2. Additional experiments on the tunneling triboelectrification mechanism

2.1 Tunneling triboelectrification by friction between the AFM tip and graphene

The potential difference between the unrubbed and rubbed region could in principle be ascribed to the friction, induced by the AFM tip, between the graphene layer and the SiO_2 layer. However, this possibility can be ruled out for the following reasons.

First, we could not obtain detectable potential differences between the rubbed and the unrubbed parts when using mechanically exfoliated graphene (MEG, see Fig. 2b and 2c), consistently with the tunneling mechanism (mechanically exfoliated graphene is clearly less defective than CVD graphene). By contrast, the hypothetical friction of mechanically exfoliated graphene with SiO_2 would likely give comparable (at least, for the orders of magnitude) results as the hypothetical friction of CVD graphene with SiO_2.

Second, the analysis of the triboelectric series for SiO_2, Pt and graphene reveals that our results may not be explained by the friction of graphene and SiO_2. In order to determine the relative positions of SiO_2 and Pt in the triboelectric series, we rubbed SiO_2 (300 nm) over a 2 × 2 μm^2 area using a grounded Pt-coated AFM tip in contact mode and measured the surface potential (5 × 5 μm^2) both before and after triboelectrification, similar to the experiments shown in Fig. 1. Supplementary Fig. 3a shows the uniform surface potential of SiO_2 before rubbing. Supplementary Fig. 3b shows that, after rubbing, the surface potential of the rubbed region decreased contrastively to results in Fig. 1c which shows an increased surface potential in the rubbed region. As a consequence, Pt is positive with respect to SiO_2 in the triboelectric series. In case of friction between Pt and graphene (Supplementary Fig. 3d), the sign of the triboelectric charges is determined by the work functions (Φ) of the two materials. In practice, after friction, electrons transfer from graphene ($\Phi_{Graphene} \approx 4.5$ eV) to Pt ($\Phi_{Pt} \approx 5.9$ eV) and then, graphene becomes positive and Pt becomes negative. The resulting triboelectric series of SiO_2, Pt, and graphene is schematically described in Supplementary Fig. 3f, so that, in the hypothetical case of friction between SiO_2 and graphene, SiO_2 would become negative and graphene positive (Supplementary Fig. 3e), contrary to our experimental results.

In conclusion, both the absence of detectable effects when using mechanically exfoliated graphene and the triboelectric series of SiO_2, Pt, and graphene confirm that the localization of charges on the insulator underneath graphene is not induced by friction between graphene and SiO_2, but is determined by the tunneling of triboelectric charges generated by friction between the Pt-coated AFM tip and graphene.

2.2 Localization of charges at the air-SiO_2 interface

In principle, the triboelectric charges might also be trapped in the defects or impurities of CVD graphene rather than being stored at the air-SiO_2 interface. In fact, this is possible during a very short transient, but this mechanism may not justify the very slow decay of the potential difference between the rubbed and unrubbed graphene areas (e.g. see Fig. 1d, 1e and Supplementary Fig. 4). Additional charges trapped in graphene defects or impurities would create potential differences in graphene, but, since CVD graphene is not insulating, these potential differences would immediately result in currents which would tend to make graphene equipotential. In CVD graphene, different from insulators, these processes would be extremely fast (i.e. in conductors or semiconductors, significant potential differences may not be maintained for long times in absence of an external perturbation). In other words, after a very fast transient, potential differences across the CVD graphene (similar to other conductors or semiconductors) would quickly disappear.

By contrast, the existence, for very long times (e.g. many days), of potential differences in graphene is easily explained by the presence of electric charges localized on an insulator underneath graphene, similar to MOS (metal-oxide-semiconductor) capacitors, the difference being that our gate is floating, immaterial, and re-writable (i.e. time variant). The localization of charges at the air-SiO_2 interface is also confirmed by the accuracy of the equivalent circuit shown in Fig. 2d, which gives reasons of the presence of a shorter time constant (associated to the discharge of the oxide capacitor) and of a longer time constant (associated to the discharge of the air-gap capacitor) as well as of the higher magnitude of the slow-decay term (almost all the charges localize on the air-gap capacitor rather than on the SiO_2 capacitor, see main text). We mention that the localization of the charges at the air-SiO_2 interface is also confirmed by the Dirac point shift (Supplementary Note 4 and Supplementary Fig. 13).

2.3 Triboelectrification of graphene on different substrates

As an additional confirmation, in order to further verify that charges are trapped at the air-gap SiO_2 interface, we also carried out identical experiments with conductive metal substrates. The CVD graphene sheet was transferred on copper (Cu) substrates was treated by HF to remove the native oxide layer (Supplementary Fig. 5). Then, the top surface of graphene was rubbed with the Pt-coated AFM tip and the surface potential was measured using KPFM. In contrast with the case of insulating substrates, triboelectric charges were not localized in the rubbed region (white dashed square) but spread to the whole region (Supplementary Fig. 5c), thus confirming that the presence of an insulator under graphene is crucial.

Moreover, we also repeated the same experiments with CVD graphene deposited on other insulating substrates such as mica and Al_2O_3 (see Supplementary Fig. 6) and, similar to the case of CVD graphene on SiO_2, found that charges, after tunneling through CVD graphene, were trapped at the interface between air-gap and SiO_2.

Supplementary Note 3. Charges stored on two series capacitors

3.1 Fundamentals on charges stored on two series capacitors

In general, series capacitors may have a non-zero net charge on their two adjacent plates (a similar situation can be found in switched-capacitor circuits where, assuming the input op amp currents can be neglected, during some periods, two capacitors can be considered as in series even if the net charge on their two adjacent plates is non-zero). For this reason, with reference to the circuit shown in Supplementary Fig. 8 it is, in general, impossible to determine the DC voltages across C_1 and C_2 (e.g. circuit simulators such as SPICE would not be able to predict the DC voltage V_X in the circuit in Supplementary Fig. 8, but would simply

warn that node X is floating).

With reference to the circuit shown in Supplementary Fig. 8, the charges associated to the capacitor C_1 are $+Q_1$ and $-Q_1$ and, similarly, the charges associated to the capacitor C_2 are $+Q_2$ and $-Q_2$. In general, we may not assume $+Q_1$ and $+Q_2$ are identical (i.e. we may not assume the net charge on the adjacent plates of C_1 and C_2, i.e. $Q_2 - Q_1$, is zero). This is certainly possible and would, in fact, be the case if, at a certain instant t_X, V_B is equal to zero and both the capacitors are fully discharged (i.e. both $+Q_1$ and $+Q_2$ equal to zero); in such case, at t_X, the net charge on the adjacent plates of C_1 and C_2, i.e. $Q_2 - Q_1$, would obviously also be zero; therefore, due to the conservation of charge, if the voltage V_B changes, since, ideally (i.e. neglecting leakage currents), no charge can flow through dielectrics, the net charge on the adjacent plates of C_1 and C_2, i.e. $Q_2 - Q_1$, will be equal to zero for ever. As a result, in this specific case, by imposing $Q_2 = Q_1$ we would find the well-known relation

$$V_X = \frac{V_B C_1}{C_1 + C_2} \tag{1}$$

Such a relation is, however, not true if the net charge on the adjacent plates of C_1 and C_2, i.e. $Q_2 - Q_1$, is different from zero.

The following fictitious experiment, schematically represented in Supplementary Fig. 9, shows that the net charge on the adjacent plates of C_1 and C_2, i.e. $Q_2 - Q_1$, can be different from zero. For simplicity, we consider ideal capacitors (e.g. we neglect leakage), ideal switches (e.g. infinite off-resistance and zero on-resistance) and two given voltages (9 V and 1V, without any loss of generality as the same discussion applies for arbitrary voltages); moreover, we assume that C_1 and C_2 are identical ($C_1 = C_2$). With such assumptions, consider the following experiment:

a) C_1 is charged to 9 V by a 9 V DC voltage source (Supplementary Fig. 9a, switches S_{1A} closed and all the other switches opened)

b) C_1 is disconnected from the DC voltage source and C_2 is charged to 1 V by a 1 V DC voltage source (Supplementary Fig. 9b, switches S_{2B} closed and all the other switches opened); the voltage across C_1 will stay constant at 9 V because C_1, after disconnection from the 9 V voltage source, is in series with an open circuit ($i = 0$) and, therefore, according to the constitutive capacitor equation $i = C\frac{dv}{dt}$, its voltage must be constant and equal to 9 V

c) All the switches are opened (Supplementary Fig. 9c) so that both the capacitor voltages will stay constant at 9 V (C_1) and 1 V (C_2), respectively (both capacitors are connected in series with an open circuit)

d) The switch S_{3C} is closed (Supplementary Fig. 9d) and, therefore, connect in series the capacitors C_1 and C_2; during this step, at all times, each capacitor is in series with an open circuit and, therefore, the voltages across both C_1 and C_2 will stay constant and equal to 9 V and 1 V, respectively, which obviously corresponds to different values for the charges Q_1 and Q_2 (we assumed $C_1 = C_2$, so if the voltages are different, the charges are different), i.e. to a net charge on the adjacent plates of C_1 and C_2, i.e. $Q_2 – Q_1$, different from zero.

3.2 Distribution of charges after tunneling triboelectrification

With reference to the two small-area series capacitors in Fig. 2d, after tunneling triboelectrification, the net charge on the adjacent plates of the two capacitors (i.e. the tunneling triboelectric charges trapped in the insulator) is certainly not zero. In fact, the existence of a significant potential difference within the graphene layer for very long times

(Fig. 1) is only possible in presence of localized charges trapped in an insulator (localized charges in both silicon and graphene would not stay localized for long times and would quickly spread out). As a result, since the net charge on the adjacent plates of the two capacitors is not zero, we may not use the relation $V_X = \frac{V_B C_1}{C_1 + C_2}$ in order to compute how the charges distribute across the small-area air gap capacitor and the small-area SiO_2 series capacitor.

However, it is easy to see that almost all the tunneling triboelectric charges, Q_{TT} (i.e. a fraction, which may be close to one in case of 1L CVD graphene, of the triboelectric charges), are stored on the small-area air gap capacitor. In fact, after tunneling through graphene, the charges Q_{TT} are trapped at the interface between air and SiO_2 and, therefore, electrostatically attract an equal amount (magnitude) of charges of the opposite type on the graphene layer and/or on the silicon underneath silicon oxide. In other words, with reference to Fig. 2d, since charges may not travel through dielectrics, the charges Q_{TT} must be stored on the top plate of the SiO_2 small-area capacitor and/or on the bottom plate of the small-area air capacitor. However, as graphically illustrated in Fig. 2d, almost all these opposite charges are attracted from graphene because of the much smaller thickness (i.e. larger capacitance) of the small-area air capacitor in comparison with the small-area SiO_2 capacitor. In fact, in order to determine the steady state (after transient) distribution of charges, only capacitors must be considered (at DC capacitors behave as open circuits which, in series with a conductive path, such as a graphene layer, dominate the impedance). Moreover, the large-area capacitors are much bigger than the small-area capacitors interested by the friction process and, therefore, dynamically behave as short circuits (i.e. the large area capacitors may be approximately seen as infinite capacitances, i.e. ideal voltage sources, i.e. equivalent, from a dynamic point of view, to short circuits). As a result, with reference to Fig. 2d, the charge Q_{TT} is shared

between the small-area air capacitor and the small-area SiO_2 capacitor as it would be shared if these two capacitors were in parallel (as both these capacitors have a terminal which, dynamically, is grounded) and therefore, similar to charge sharing in parallel capacitors, most charges accumulate across the larger capacitance (i.e. the small-area air capacitor). As a consequence, the charges stored on the small-area SiO_2 capacitor are almost unaffected by tunneling triboelectrification and, therefore, the voltage drop across the small-area SiO_2 capacitor is also almost unchanged (i.e. stays at zero) so that the voltage drop measured across graphene by KPFM is almost identical to the voltage drop across the small-area air gap capacitor.

As a result, by considering the air gap thickness t_{Air} (Supplementary Fig. 2), we easily estimate the charge density (Fig. 3e) stored underneath graphene in (x,y) as $\frac{\varepsilon_{Air}\Delta V_{TT}(x,y)}{t_{Air}}$

where ΔV_{TT} is the surface potential measured (by KPFM) in the point (x,y) taken with reference to the average surface potential of the unrubbed region (see main text), $\varepsilon_{\mathrm{Air}}$ is the dielectric constant of air and t_{Air} is the thickness of air gap.

3.3 Decay time of ΔV_{TT}

In the hypothetical circuit shown in Supplementary Fig. 10a, the two capacitors C_1 and C_2 are in parallel (each capacitor connects the same couple of terminals). The two parallel capacitors C_1 and C_2 could, therefore, also be represented as a single capacitor with capacitance C_1+C_2; as a result the discharge of the capacitors would be exponential with a single time constant equal to $(R_1//R_2)(C_1+C_2)$, where $R_1//R_2$ is the parallel of R_1 and R_2, i.e. $R_1R_2/(R_1+R_2)$.

However, in case of tunneling triboelectrification, after the equilibrium has been reached, there is no current across graphene, thus resulting in the equivalent circuit shown in

Supplementary Fig. 10b. As a consequence, due to Kirchoff's current law (i.e. conservation of charge), there may be no current going from the top bipole (parallel connection of R_1 and C_1) to the bottom bipole (parallel connection of R_2 and C_2). Therefore, the capacitor C_1 may only discharge through the resistor R_1, thus resulting in a time constant R_1C_1; similarly, the capacitor C_2 may only discharge through the resistor R_2, thus resulting in a time constant R_2C_2, in perfect agreement with our experiments (e.g. see the excellent agreement between experimental points and the best fit in Fig. 1e). As a result, the total voltage (measured by KPFM) will evolve with time as

$$\boldsymbol{v}(\boldsymbol{t}) = \boldsymbol{V}_1\boldsymbol{e}^{\frac{-\boldsymbol{t}}{\tau_1}} + \boldsymbol{V}_2\boldsymbol{e}^{\frac{-\boldsymbol{t}}{\tau_2}} \quad (2)$$

where V_1 is the initial voltage (at $t = 0$) across C_1, V_2 is the initial voltage (at $t = 0$) across C_2, $\tau_1 = R_1C_1$, and $\tau_2 = R_2C_2$.

In practice, in case of tunneling triboelectrification, one of these two addends dominates at all times as it has both a higher initial magnitude and a longer time constant. In fact, the higher initial magnitude is certainly associated to the air gap capacitor because almost all the tunneling triboelectric charges are localized across the air gap capacitor (see main text and Supplementary Note 3.2); additionally, air is a much better insulator than silicon oxide and, therefore, the time constant associated to the air gap capacitor is much longer than the time constant associated to the SiO_2 capacitor.

These results are in perfect agreement with all our experiments and give reasons for the exceptionally long time constants we found after tunneling triboelectrification (more than two orders of magnitude longer than for conventional triboelectrification of a dielectric).

Supplementary Note 4. Control of CVD graphene devices by ghost floating gates

4.1 Resistance control on CVD graphene resistor

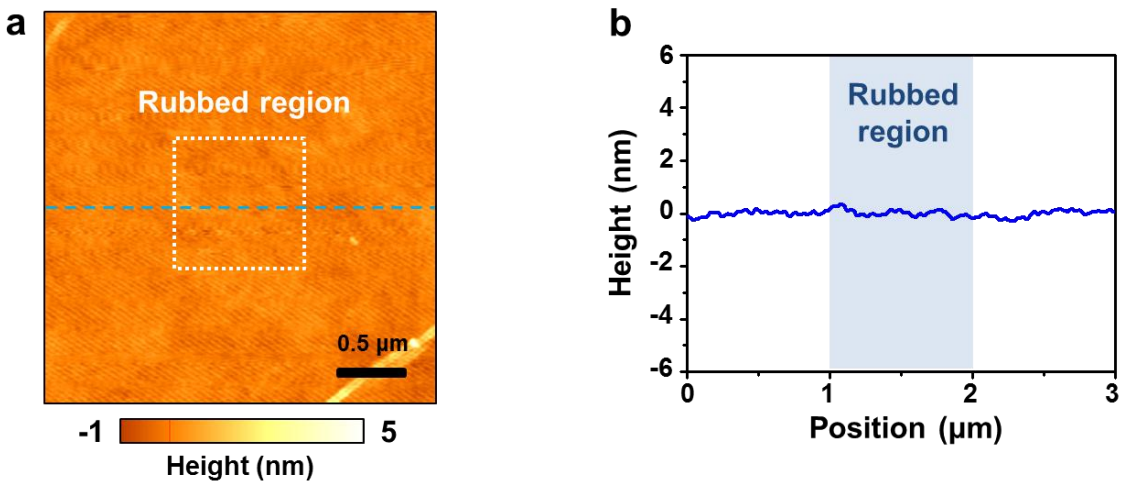
Supplementary Fig. 12 shows the resistance reduction induced on the 4-contacts 1L CVD graphene resistor shown in Fig. 4. In practice, as schematically shown in Supplementary Fig. 12a, we performed 4-wires measurements by injecting a 100 nA current through the force electrodes F_1 and F_2 and measuring the voltage difference across the inner sense electrodes S_1 and S_2 (the instrumentation amplifier *IA* has negligible input currents and, therefore, first, the entire I_0 current flows through the graphene resistor R_G, and, second, the voltage across the input terminals of the instrumentation amplifier is exactly the same as the voltage across R_G). For instance, Supplementary Fig. 12b-d show the voltages across R_G (i.e. 100 nA × R_G) before (higher value of R_G and, therefore, of the voltage difference across R_G) and after rubbing the middle area (yellow dashed box, between the sense electrodes S_1 and S_2 in Fig. 4a) with an AFM-Pt tip biased at -10 V (b), -5 V (c), and 0 V (d), respectively. As evident, the tunneling triboelectric charges act as ghost floating gates and electrostatically reduce the normalized resistance R/R_0 (where R is the resistance of graphene after rubbing and R_0 is the resistance before rubbing). These results already constitute a device-level demonstration of tunneling triboelectrification (e.g. tunable resistors are useful in tunable amplifiers, automatic gain control circuits, tunable voltage/current references, etc.).

4.2 Dirac point shift by tunneling triboelectrification

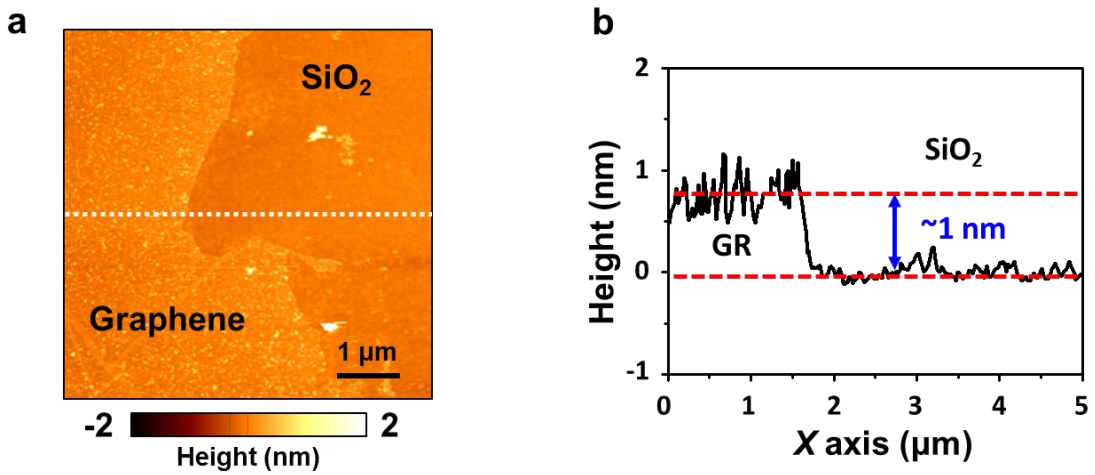
In addition to the control of graphene resistivity by tunneling triboelectrification (Fig. 4 and Supplementary Fig. 12), we also verified that tunneling triboelectrification allows to control the Dirac point of graphene (Supplementary Fig. 13). In practice, we measured the drain-to-source current (I_{DS}) of a graphene resistor as a function of the back gate voltage (V_{BG}) both

before and after rubbing p-doped graphene with an AFM tip biased at +10 V. The I_{DS}-V_{BG} curves were measured under constant drain-to-source voltage (V_{DS} = 0.01 V). As described in Supplementary Fig. 13b, after tunneling triboelectrification, the Dirac point of the graphene resistor shifts to the left and, with a zero gate voltage, the effective doping turns from p-type to n-type. In fact, consistently with our theoretical discussions, first, positive charges are generated in graphene by triboelectrification with the positively biased AFM tip and, second, part of these positive charges tunnel through the air gap and effectively turn the naturally p-type graphene into n-type (Supplementary Fig. 13a). This situation is exactly the same found in MOS (metal-oxide-semiconductor) capacitors where the presence of charges on the metal gate induces opposite charges on the semiconductor and, therefore, travelling through the semiconductor at the semiconductor-oxide interface, going from the region underneath the gate to the surrounding regions of the semiconductor, there are potential differences (due to the gate charges) which may be well preserved for very long times. This is exactly analogous to our case, the difference being that our gate is floating, immaterial, and re-writable (or, equivalently, time variant). In conclusion, Supplementary Fig. 13b confirms that tunneling triboelectrification can effectively control the current transport characteristics of 2D devices.

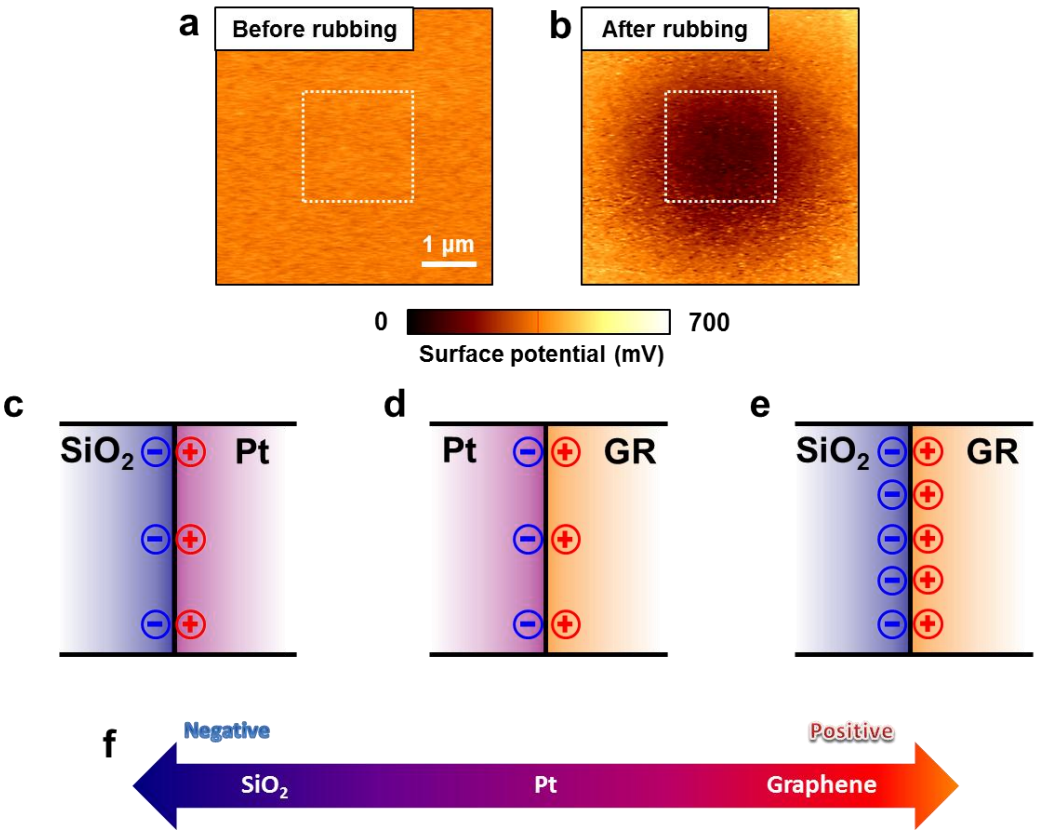
We mention that Supplementary Fig. 13b also provides an additional confirmation that the positive charges induced on graphene by rubbing with the positively biased AFM tip (+10 V) tunnel through the air gap and localize at the SiO_2-air interface; in fact, such localized positive charges electrostatically attract free charges of the opposite type (negative) in graphene (i.e. turn graphene from p-type to n-type doping), similar to what would happen with positive charges localized on an hypothetic gate underneath the air-gap.



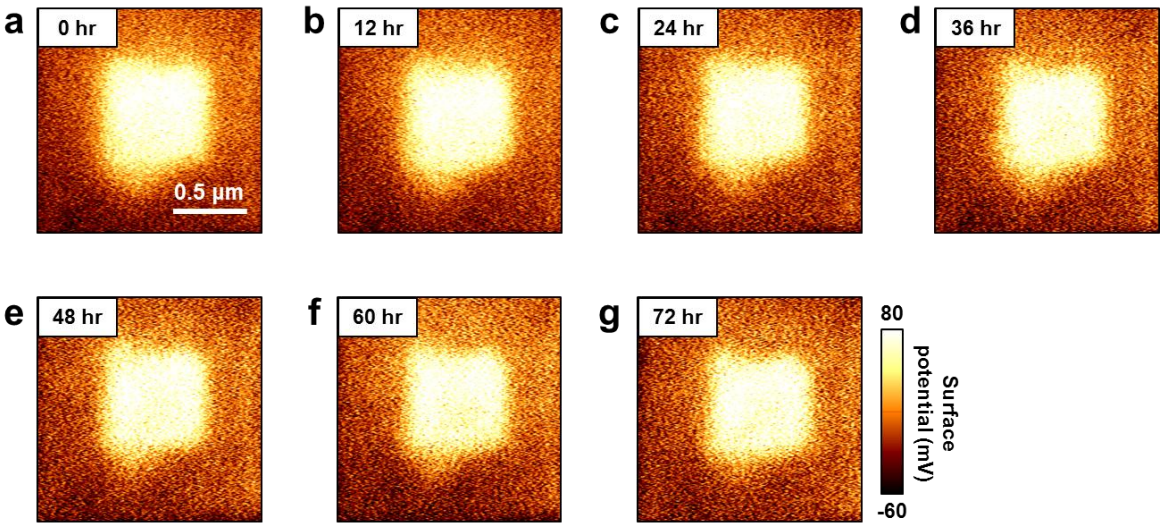
Supplementary Figure 1 | Absence of damages in CVD graphene after rubbing with the Pt AFM tip. (**a**) Topography image of CVD graphene after rubbing. The white box indicates the rubbed region. (**b**) Cross-sectional profile along the blue dashed line in (**a**).



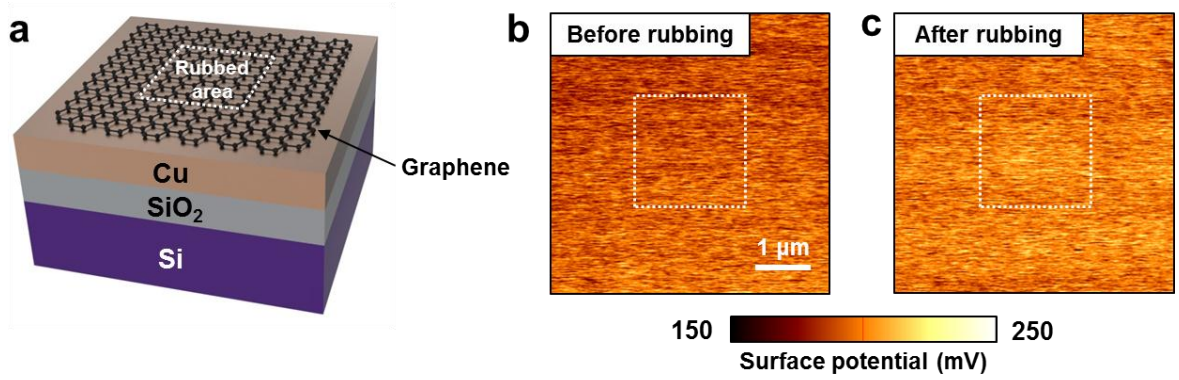
Supplementary Figure 2 | **AFM measurement of the air gap thickness.** The step is about 1 nm, so that, taking into account the 0.34 nm thickness of monolayer graphene, the air gap thickness can be estimated around 0.66 nm. (**a**) Topography image of CVD graphene on SiO_2. (**b**) Cross-sectional profile along the white dashed line in (**a**).



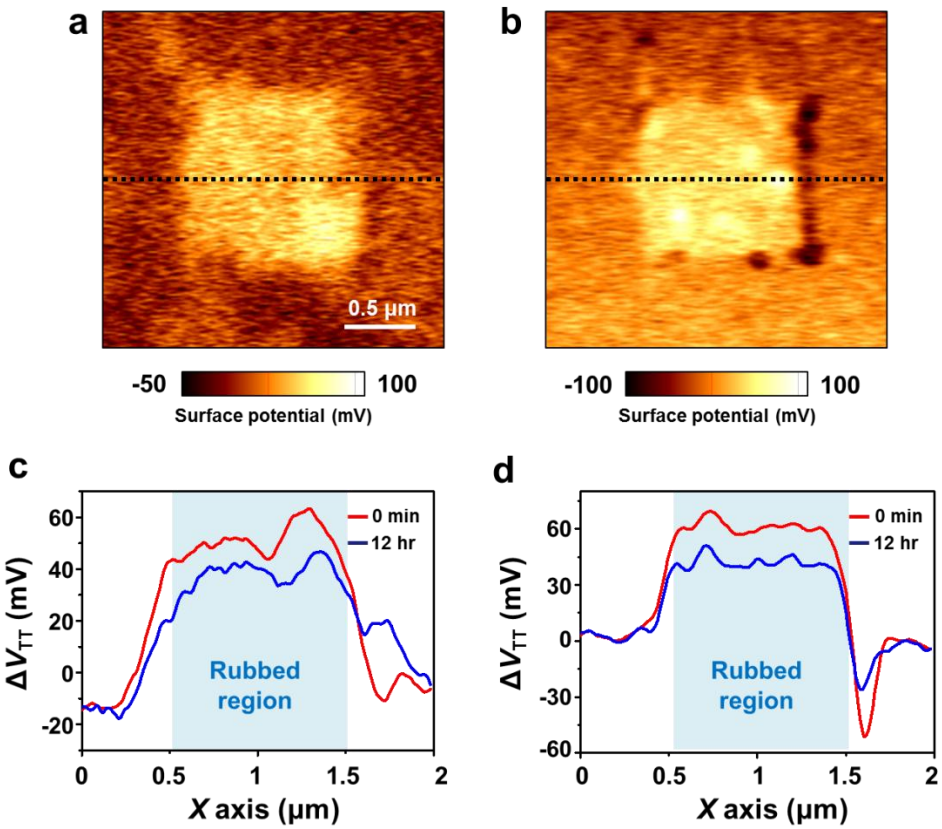
Supplementary Figure 3 | Triboelectric series of SiO_2, Pt and graphene. (**a**) KPFM image of SiO_2 before and (**b**) after rubbing with Pt-coated AFM tip. (**c**)-(**e**) Schematic representation of the triboelectric charge transfer processes in (**c**) SiO_2/Pt, (**d**) Pt/graphene and (**e**) SiO_2/graphene. (**f**) Triboelectric series of SiO_2, Pt and graphene.



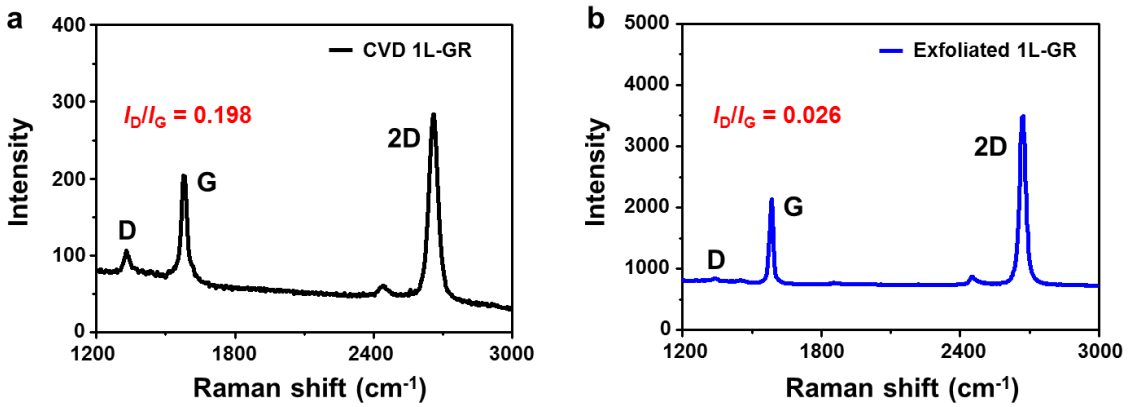
Supplementary Figure 4 | KPFM images taken at different times after rubbing 1L CVD graphene. (**a**)-(**g**) The localized triboelectric charges were very well preserved under the rubbed region even after 72 hours.



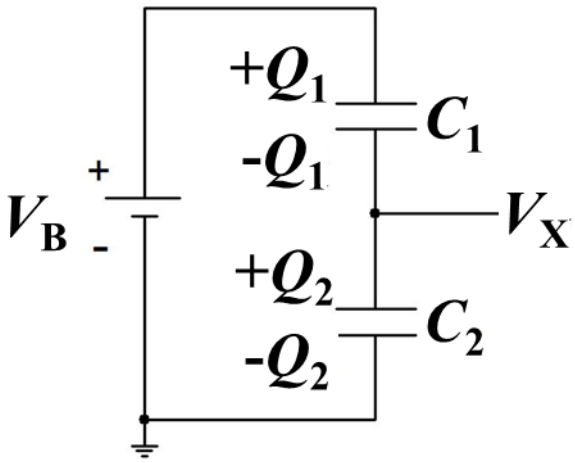
Supplementary Figure 5 | Triboelectrification of graphene on metal substrate. (**a**) Schematic image of graphene transferred on metal (Cu) substrate. (**b**) KPFM image of graphene on metal substrate before rubbing and (**c**) after rubbing with Pt-coated AFM tip.



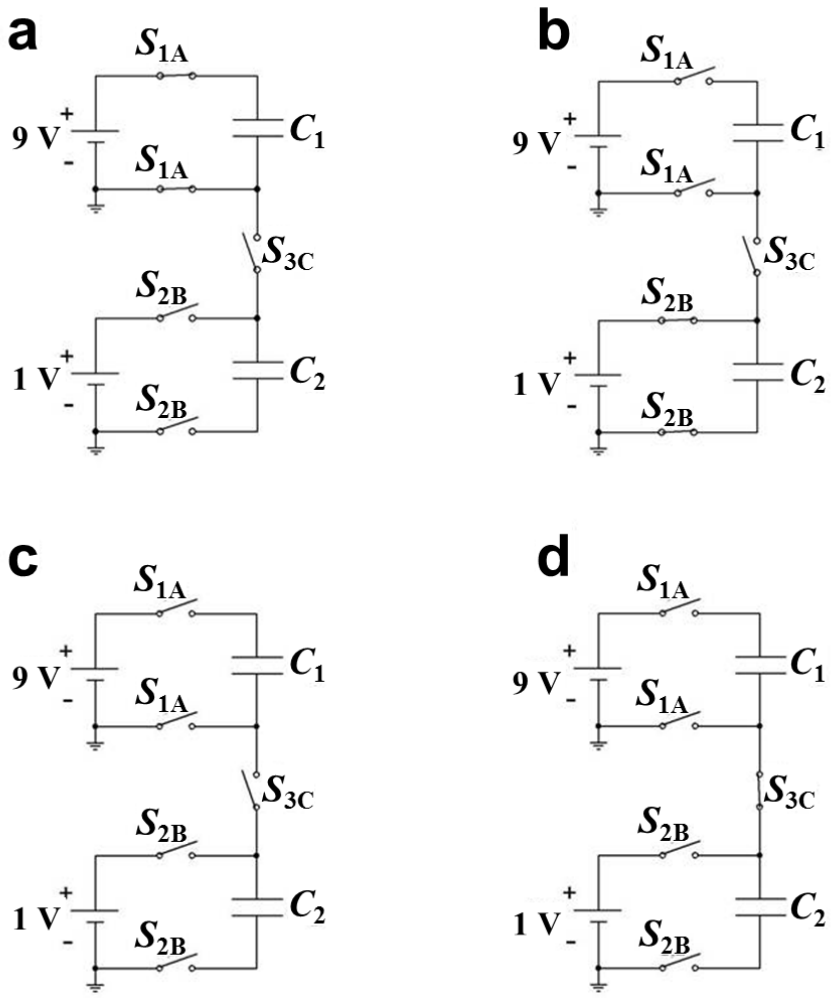
Supplementary Figure 6 | Tunneling triboelectrification of graphene on mica and on Al_2O_3. (**a**), (**b**) KPFM images, after tunneling triboelectrification, of CVD graphene deposited on (**a**) Mica and CVD graphene deposited on (**b**) Al_2O_3. (**c**), (**d**) Cross-sectional profiles along the black dashed lines for graphene on (**c**) Mica and graphene on (**d**) Al_2O_3 after 0 min and 12 hours.



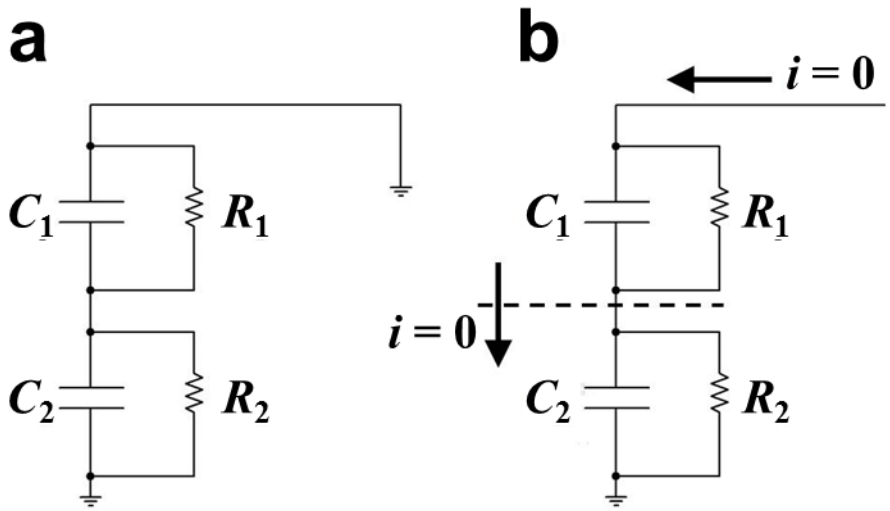
Supplementary Figure 7 | Raman spectra of 1L CVD graphene and mechanically exfoliated 1L graphene. (**a**) Raman spectra of 1L CVD graphene. (**b**) Raman spectra of exfoliated 1L-graphene, showing D, G, 2D peaks at ~ 1300, ~ 1600 and ~ 2700 cm^{-1} respectively. The ratios of I_G/I_{2D} = ~ 0.5 in (**a**) and (**b**) show that they are mono-layer graphene. The ratios of I_D/I_G = 0.198, 0.026 for CVD graphene and exfoliated graphene, respectively, show that the CVD graphene has a lot of defect regions compared to the exfoliated graphene (Renishaw, RM-1000 Invia, 514 nm, Ar^+ ion laser).



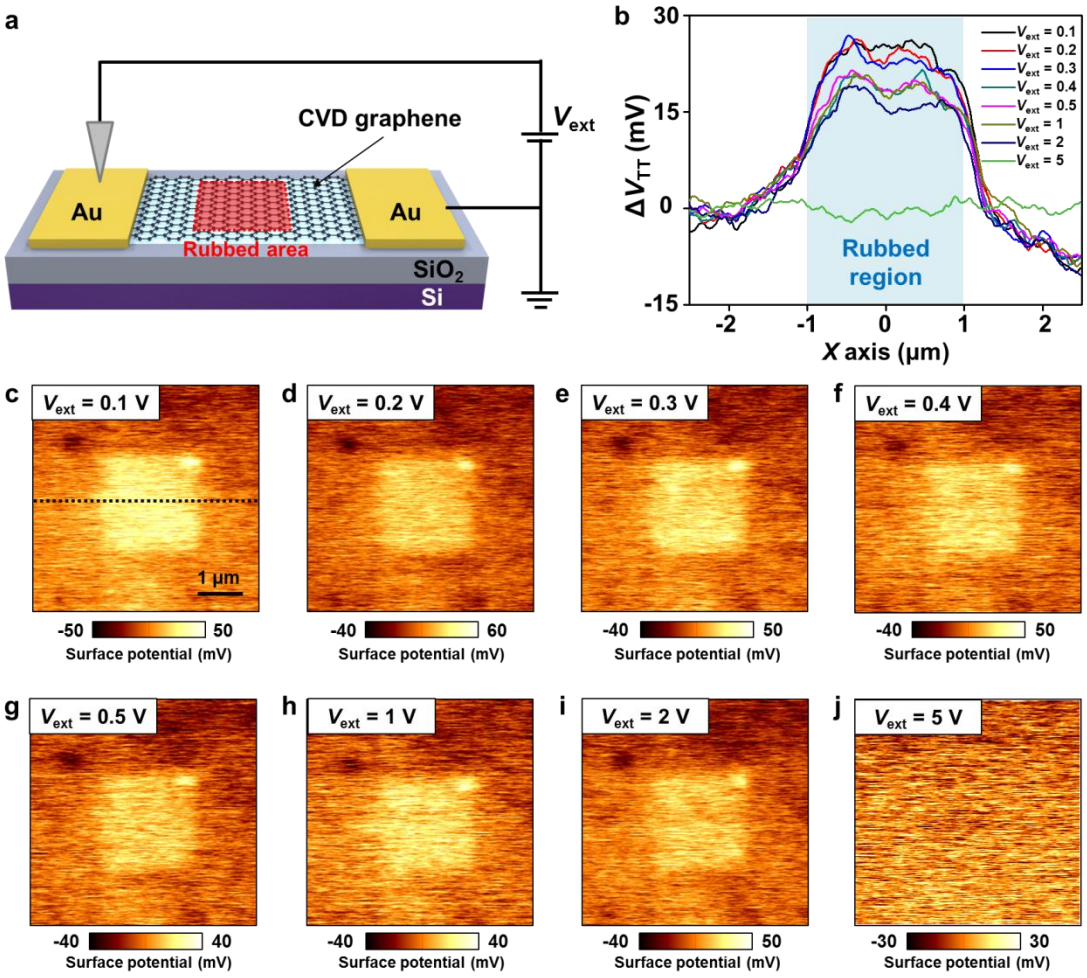
Supplementary Figure 8 | Circuit for illustrating how charges distribute on two capacitors in series.



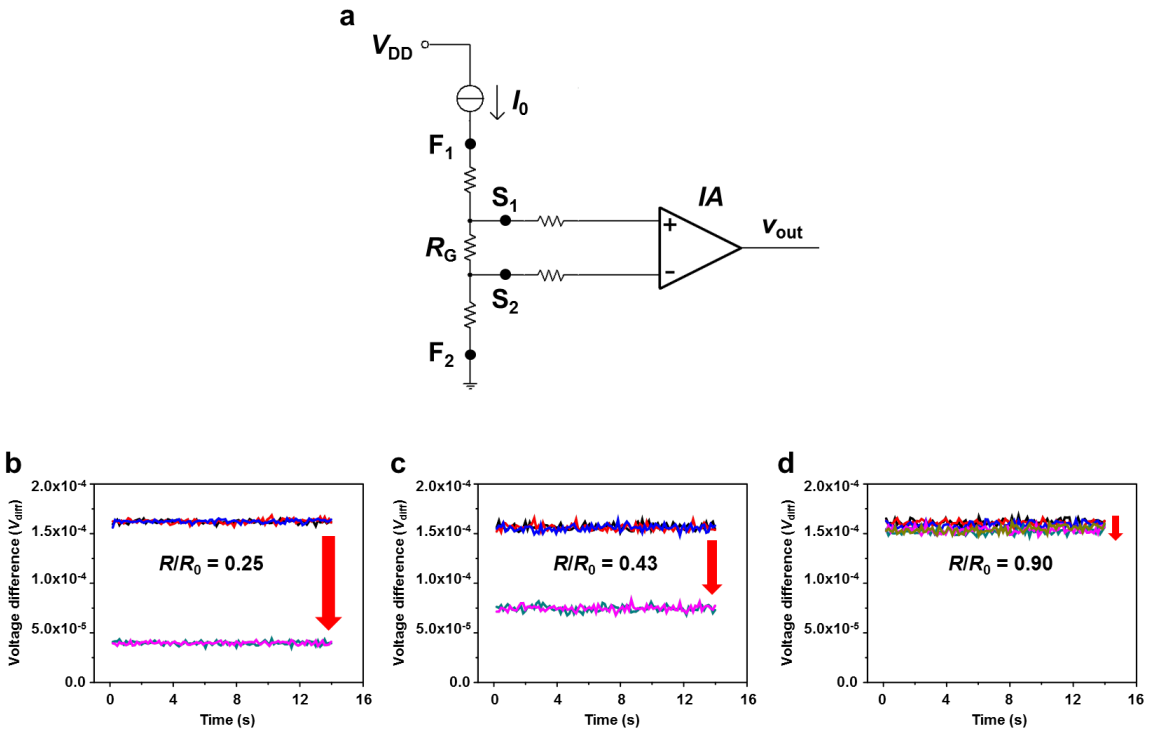
Supplementary Figure 9 | Fictitious experiment illustrating that two arbitrary charges can be stored on two series capacitors. (**a**) C_1 is charged at 9 V. (**b**) C_2 is charged at 1 V, the voltage across C_1 is constant because $i_{C1} = C\frac{dv_{C1}}{dt} = 0$. (**c**), (**d**) The voltages across C_1 and C_2 are constant because $i_{C1} = C\frac{dv_{C1}}{dt} = 0$ and $i_{C2} = C\frac{dv_{C2}}{dt} = 0$, respectively.



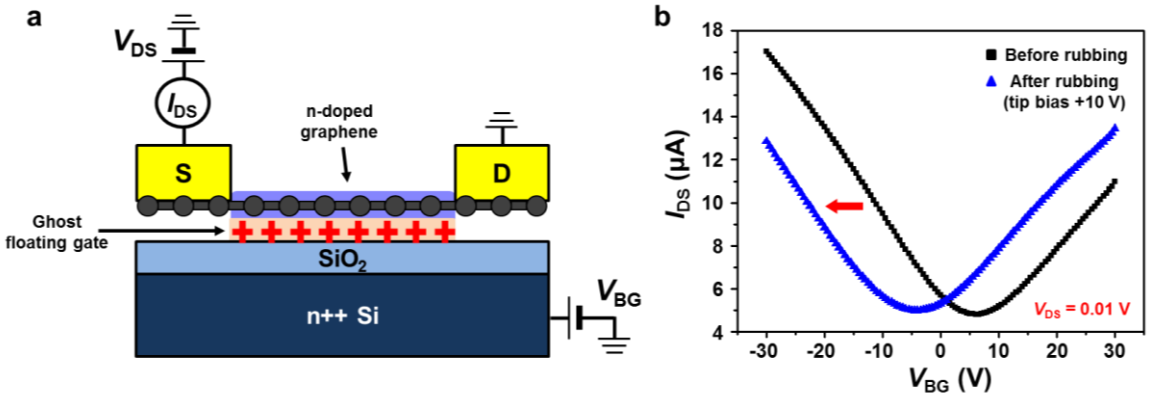
Supplementary Figure 10 | Discharge of capacitors in different configurations. (**a**) For two capacitors in parallel, each one with a resistance in parallel, the decay is exponential with a single time constant equal to $\left(\boldsymbol{R}_1 // \boldsymbol{R}_2\right)\left(\boldsymbol{C}_1 + \boldsymbol{C}_2\right)$. (**b**) Equivalent circuit for the decay of the voltage ΔV_{TT}; since the current through the graphene layer is zero, each capacitor exclusively discharges through its parallel resistor, resulting in two distinct time constants $\boldsymbol{R}_1\boldsymbol{C}_1$ (associated to the air gap capacitor) and $\boldsymbol{R}_2\boldsymbol{C}_2$ (associated to the SiO_2 capacitor).



Supplementary Figure 11 | Trapped charges survive even under relatively high currents flowing through the rubbed graphene. (**a**) Schematic image of the device structure; after rubbing, the AFM tip is used to apply an external voltage for 7 minutes and induce currents in the mA range. (**b**) Cross-sectional profiles along the black dashed line in (**c**) to (**j**). These profiles clearly show the remaining of tunneling triboelectric charges even after applying the external voltage up to a certain threshold. (**c**) to (**j**) KPFM images after applying an external voltage V_{ext} (0.1 ~ 5 V) on CVD graphene which has localized charges under graphene (bright region in the center of the CVD graphene). The localized tunneling triboelectric charges were well preserved after applying V_{ext} = 2 V, but were completely erased after applying V_{ext} = 5 V.



Supplementary Figure 12 | Resistance reduction of graphene by tunneling triboelectrification. (**a**) Schematic representation of 4-contacts 1L CVD graphene resistor and of the 4-wires measurement technique. (**b**)-(**d**) Voltages measured across the sense terminals S_1 and S_2 with I_0 = 100 nA before and after AFM tunneling triboelectrification performed with tip bias voltages of (**b**) -10 V, (**c**) -5 V, (**d**) 0 V.



Supplementary Figure 13 | Control of the Dirac point by tunneling triboelectrification. (**a**) Schematic image of the device structure and of the ghost floating gate. (**b**) I_{DS}-V_{BG} curves before (black) and after (blue) tunneling triboelectrification (V_{DS} = 0.01 V).

Supplementary References

1. Lee, C., Wei, X., Kysar, J. W. & Hone, J. Measurement of the elastic properties and intrinsic strength of monolayer graphene. *Science* **321,** 385-388 (2008).

2. Geim, A. K. Graphene: status and prospects. *Science* **324,** 1530-1534 (2009).