Gate–Source Distance Scaling Effects in H-Terminated Diamond MESFETs

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***Abstract*— In this paper, an analysis of gate–source and gate–drain scaling effects in MESFETs fabricated on hydrogen-terminated single-crystal diamond films is reported. The experimental results show that a decrease in gate–source spacing can improve the device performance by increasing the device output current density and its transconductance. On the contrary, the gate–drain distance produces less pronounced effects on device performance. Breakdown voltage, knee voltage, and threshold voltage variations due to changes in gate–source and drain–source distances have also been investigated. The obtained results can be used as a design guideline for the layout optimization of H-terminated diamond-based MESFETs.**

***Index Terms*— Diamond, MESFETs, output current, semiconductor device manufacture, transconductance.**

I. Introduction

DIAMOND is a semiconductor material featured by outstanding physical, mechanical, and chemical properties if compared with other semiconductors widely adopted in electronic device fabrication, e.g., Si, GaAs, 4H-SiC, and GaN. Wide-bandgap (5.5 eV), high breakdown electric field (10 000 kV/cm), low dielectric constant (5.7), high thermal conductivity (22 $W/cm \cdot K$), and high electron saturation velocity ($2.7 \cdot 10^7$ cm/s) are the examples of its distinctive physical properties [1], [2]. Diamond is thus expected to be suitable for the fabrication of high-power and high-frequency electronic devices for applications in many different fields, such as in communication satellites and radars. This has pushed research groups worldwide to realize electronic devices on single- and poly-crystalline diamond films aimed at demonstrating such suitability [3]–[5]. The p-type conductive characteristics of hydrogen-terminated diamond surface were reported in [6] and its application to a FET device was first demonstrated in [7]. A hole accumulation in the subsurface region is originated by the energy band bending due to the interaction of hydrogen-terminated diamond surface with adsorbed ions also present in the atmosphere. In this way, the 2-D hole gas (2-DHG) is formed only below the H-terminated surface and is used as an active channel in FET devices.

Diamond MESFET realization relies on a few technological steps. In particular, device performance is mainly dependent on crystal quality of grown diamond films and its surface termination, metal/diamond junction characteristics, and geometrical factors. In this respect, a large number of diamond MESFET structures and various optimizations have been reported in [8]–[10]. Among them, the influence of the crystalline and surface properties of the homoepitaxial diamond layer has been analyzed in [11]. The effects of device passivation (e.g., with Al_2O_3, AlN, and MO_3) have been also studied [12]–[18] to overcome the thermal instabilities and drifts from which the surface channel of diamond MESFETs suffers. In addition, enhancement and stabilization of hole concentration in hydrogen-terminated diamond surface have been reported using different gas species (e.g., O_3, NO_2, and NO) and MO_3 deposition [16]–[19]. Finally, the scaling effect of gate length on the RF and dc performance of hydrogen-terminated diamond FETs have been studied [9], [20], [21].

The peculiar transport characteristic of diamond still offers the possibility to enhance the device performance by proper geometry optimization. For instance, Russo and Di Carlo [22] reported the simulation results on the effects of scaling gate–source (L_{GS}) and gate–drain (L_{GD}) distances, as well as gate length (L_G), in GaN-based HEMTs, whereas Deng *et al.* [23] carried out a similar theoretical study on SiC MESFETs. In the references above, the current density increase in the active channel associated to a reduction of the gate–source distance is shown to be due to the peculiar velocity-field characteristics of GaN or SiC semiconductors, in which the ohmic (linear) regime extends up to electric fields in the order of 100 kV/cm [23], [24]. Such a physical property can be transposed to diamond devices, characterized by saturation electric fields [25] close to the values reported for GaN and SiC. To the best of the authors' knowledge, such study has not been performed yet on H-terminated diamond MESFETs.

The aim of this paper is to investigate, through an extensive measurement campaign, the dc performance of H-terminated

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diamond devices as a function of geometric parameters L_{GS} and L_{GD}. A description of the adopted single-crystal diamond growth procedure is given first. The diamond MESFET fabrication process is then briefly addressed, describing the realized device geometries. Finally, a description of the adopted test bench and the measurements performed on the samples with different geometries are presented, and the results are discussed.

II. CVD Single-Crystal Diamond Growth

A high-quality single-crystal diamond film with a thickness of about 2 μm was homoepitaxially grown by microwave plasma-enhanced chemical vapor deposition (CVD) on a $4.5 \times 4.5 \times 0.5$ mm^3 commercial low-cost synthetic high-pressure high-temperature 1b-type diamond (1 0 0) substrate polished on one side. No dopants were intentionally added during the deposition process. Nevertheless, the presence of an acceptor concentration of the order of 10^{14} cm^{-3} has been observed in [26] using diamond samples grown in the very same deposition conditions.

Prior to fabricating the devices, the diamond surface has been terminated with hydrogen (H-termination) to form a p-type channel. H-surface termination was performed by exposing the diamond surface to H plasma *in situ*, i.e., in the same microwave CVD reactor, at the end of the growth. In particular, the following two-step procedure was adopted: 1) the deposited diamond film was exposed to a hydrogen plasma for 20 min and 2) after the microwave power switch-OFF, the sample was cooled down to room temperature in a pure hydrogen atmosphere.

The surface morphology study was performed by an atomic force microscope in contact mode with the CVD diamond sample. A homogeneous surface with an average roughness of about 5-nm rms over 10-μm area was observed. It is worth pointing out that the diamond surface was free of defects such as pyramidal hillocks, flat hillocks, and unepitaxial crystallites.

Four Au ohmic contacts were then evaporated in the van der Pauw configuration for Hall measurements at room temperature in air. A surface carrier density and a hole mobility of about $1.1 \cdot 10^{13}$ cm^{-2} and 110 cm^{2}V^{-1}s^{-1} were measured, respectively. In addition, the electrical properties of Au/H-terminated diamond contacts were investigated by current–voltage (I–V) measurements at room temperature in air. A sheet resistance of about 6.5 kΩ/sq and an ohmic contact resistance of 4 $\Omega \cdot$ mm were obtained by the transmission line method.

III. MESFET Device Fabrication Process and Device Characterization

The devices were realized on the CVD diamond homoepitaxial layer by exploiting the following fabrication process.

A 200-nm Au film was thermally evaporated on the H-terminated diamond surface and used for source and drain ohmic contacts. A polymethyl methacrylate resist, covering the device area, was patterned by a first electron-beam lithography (EBL) step and used as mask for wet etching of gold by KI/I_2. To electrically insulate the devices on the same diamond substrate, the diamond surface exposed was oxidized by reactive ion etching (RIE) in a low-energy Ar and O_2 plasma gas mixture. The isolation was established to force the drain–source current to flow underneath the gate, thereby avoiding parasitic resistive effects. The RIE treatment used to electrically isolate the devices exhibits a diamond surface etching depth of about 1.5 nm.

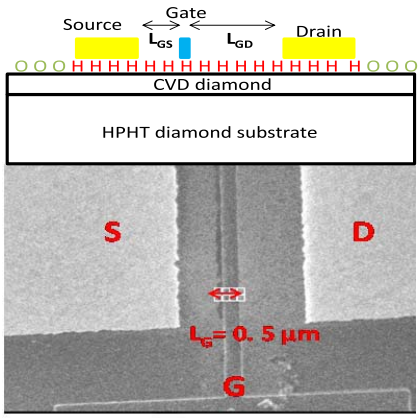

Fig. 1. Top: sketch of the device structure. Bottom: SEM picture of a typical channel geometry.

To realize the drain–source channel of the MESFETs, a second EBL step was performed, followed by the Au wet chemical etching that gives rise to the separation between the source and drain contacts.

Finally, an aluminum Schottky contact (150-nm thick) was used as gate electrode. To place the gate in the channel at different distances from source and drain contacts, a third EBL step was used. The gate fabrication process finished with electron gun evaporation of aluminum and lift-off technique.

A sketch of a diamond MESFET device cross section and a scanning electron microscope (SEM) image of the device active area are shown in Fig. 1.

Many devices were fabricated on the same substrate, each of which is featured by a single gate finger with 0.5-μm width (L_G) and 50-μm length (W), whereas L_{GS} and L_{GD} vary as detailed in the following. To maximize the number of devices per geometry on the substrate, a compact simplified layout, accessible via three dc pads, has been devised. The devices can then be easily tested by choosing, according to the need, which pad is to be used as the source/drain. As a consequence, the range of available L_{GS}, L_{GD} pairs is expanded by simply inverting the supply scheme applied to a relatively small set of fixed geometries.

Realized devices can be grouped in two sets: in the first one, the total drain–source length was kept fixed ($L_{DS} = L_{GS} + L_G + L_{GD} = 6.5$ μm) while varying the gate finger position; in the second set, the gate–source (gate–drain) distance was varied in the range 1.0–2.6 μm while keeping the gate–drain (gate–source) distance fixed to

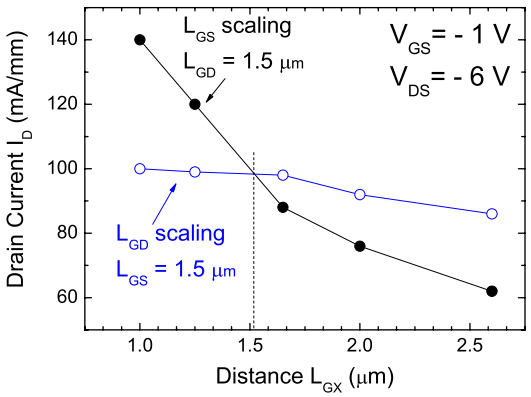

Fig. 2. Drain current density as a function of L_{GS} and L_{GD} distances. Gate width is 50 μm. Gate length is 0.5 μm.

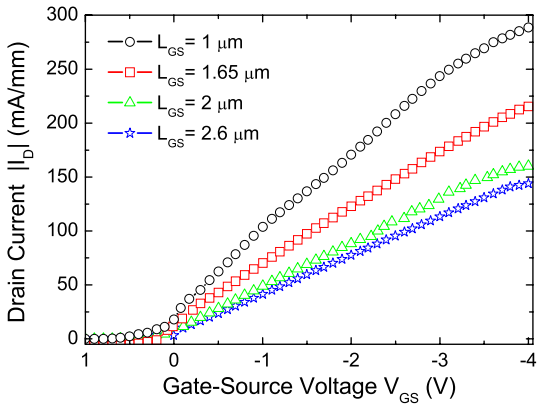

Fig. 3. Drain current density as a function of V_{GS}, with L_{GS} as a parameter, for $V_{DS} = -6$ V.

about 1.5 μm (therefore, changing also the total drain–source length).

All devices have been characterized under different bias conditions to identify some key parameters or to test the devices till the occurrence of the device breakdown. Measurements have been performed using a Cascade Microtech RF-1 probe station, jointly with three dc micropositioners to properly handle and contact the devices under test. DC measurements have been performed with a proprietary LabVIEW software in conjunction with a Hewlett Packard power supply (6622A) and four Hewlett Packard multimeters (34401A), two configured as voltmeters and the remaining as ampmeters. Breakdown tests have been performed with a Keithley (model 6517B) electrometer.

IV. Results and Discussion

Drain current density as a function of L_{GS} and L_{GD} and measured in a fixed bias condition, namely, $V_{GS} = -1$ V and $V_{DS} = -6$ V, is shown in Fig. 2. Scaling L_{GD} has nearly no effect on the current density, in contrast with the L_{GS} scaling, which has a noticeable impact on drain output current density. In particular, the latter increases by a factor of about 2.3 when the L_{GS} distance is shortened from 2.6 to 1.0 μm.

This behavior has already been theoretically predicted in other wide-bandgap semiconductor technologies, such as GaN-HEMT [22] and 4H-SiC MESFETs [23]. Russo and Di Carlo [22] and Deng *et al.* [23] supported from 2-D device simulations discuss the gate–source distance scaling effect by considering the peculiar velocity-field characteristics of GaN and 4H-SiC materials. The key feature, as already mentioned, is the ohmic regime extending up to about 100 kV/cm [23], [24]. More in detail, the downscaling of L_{GS} enhances the electric-field component along the channel between source and gate (E_{GS}) and, proportionally, the average carrier velocity in the same region. Assuming the carrier density between source and gate is approximately constant (also with respect to L_{GS}), the effect is an increased current density, which flows all the way to the drain. However, in the gate–drain region, much higher applied fields (at least one order of magnitude higher) take place in normal operation so that carrier velocity reaches the saturation value. In conjunction with this phenomenon, charge conservation imposes an increase in the carrier density, which indeed is maximum under the gate metallization, as verified in [22] and [23]. As a result, the E_{GS} increase produced by downscaling L_{GS} boosts the current density in saturation. Conversely, the downscaling of L_{GD} does not produce any increase in the electric field in the source–gate region, thus not affecting the saturated drain current. On the basis of [25], a similar behavior should be expected for H-terminated diamond devices. In [25], in more detail, the threshold fields for the onset of the nonlinear carrier velocity regime are shown, both for bulk and surface holes. Threshold values in the range 10–100 kV/cm have been reported, where the lower bound is associated with bulk holes and a low level of impurities per volume, whereas the upper bound is associated with bulk holes and a high level of impurities per volume or, equivalently, with superficial holes in the 2-DHG.

The drain current density measured for a fixed drain–source voltage ($V_{DS} = -6$ V) as a function of the applied gate–source voltage is reported in Fig. 3 for different L_{GS}, whose value is ranging from 1.0 to 2.6 μm.

The drain current (I_D) measured in Fig. 3 is about 20% less than that reported in Fig. 2 at the same bias point. Repeated measurements of dc drain I–V (I_D–V_{DS}) characteristics show that drain current decreases appreciably due to channel degradation. This phenomenon has already been reported in [4] and [21] for diamond-based MESFETs.

It can be observed that L_{GS} scaling only affects the slope of the transcharacteristics. The threshold voltage is only slightly influenced and is estimated to be about +0.3 V in all cases. At $V_{GS} = -4$ V, the transcharacteristics start bending down, implying that the maximum attainable current density is probably only slightly higher than the one achieved at −4 V. This is consistent with the rapid decrease in the dc transconductance, g_m, shown in Fig. 4 for V_{GS} values lower than 2.5 V. In Fig. 4, the positive impact on the transconductance values when downscaling L_{GS} is also evident: a decrease in L_{GS} from 2 to 1 μm results in an increase in g_m from 40 to 85 mS/mm.

The double-hump shape clearly shown in Fig. 4 by the transconductance associated to the smallest L_{GS} has already

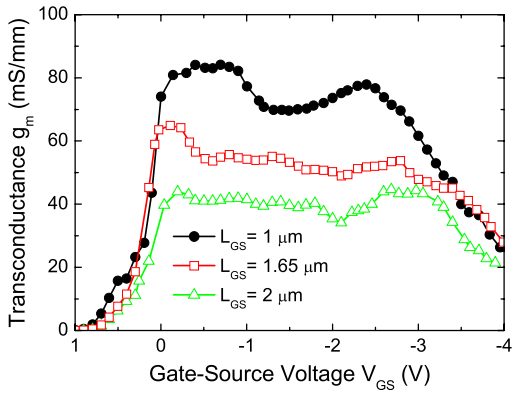

Fig. 4. DC transconductance per unit gate width as a function of V_{GS}, with L_{GS} as a parameter, for $V_{DS} = -6$ V.

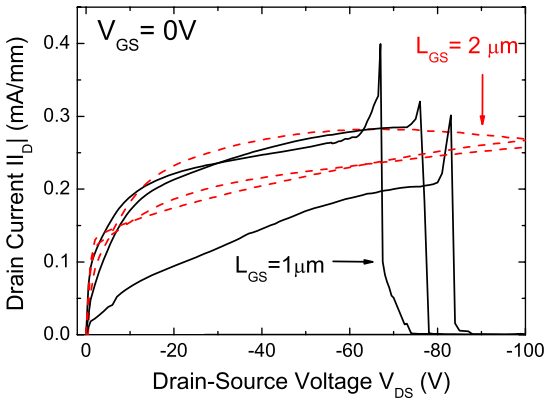

Fig. 5. Drain current density as a function of V_{DS}, for $V_{GS} = 0$ V, for breakdown voltage evaluation.

been observed in [27]–[29] and may evoke the behavior of a double-channel device [30], [31]. It is therefore worth noting that in the present case of H-terminated diamond FETs, a single 2-DHG was sought, and no intentional measures were taken to produce an additional channel. As a consequence, it is not possible to establish with sufficient confidence what effect originates the observed double hump: this topic may deserve further investigation on the basis of advanced physical simulations. At any rate, physical models presented so far in [25], [32], and [33] are not suited to predict the observed transconductance humps.

It is worth to mention that gate current leakage, constantly monitored during the whole measurement campaign, never exceeded values as low as 7 μA/mm (worst case taken at $V_{GS} = -3.2$ V and $V_{DS} = -15$ V). Furthermore, no evident dependences of gate leakage on gate–source or gate–drain distances were observed.

Although this paper is aimed at understanding the dc properties of H-terminated diamond devices as the gate–source distance is scaled down, some remarks about the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) as functions of scaling can be done as well. In particular, the equation correlating transconductance to the intrinsic FET cutoff frequency, $f_T = g_m/2\pi C_{gs}$, may let the reader infer that f_T increases proportionally to g_m. However, the increase in the electron density under the gate actually reduces the size of the pinchoff region at the drain end of the gate. This results in an increase in the gate capacitance (C_{gs}) so that the g_m/C_{gs} ratio stays nearly constant. Such a conduction mechanism in the channel is very similar to what observed in GaN and 4H-SiC devices, with the only exception that holes rather than electrons are the carriers involved in the case of H-terminated diamond-based FETs. Indeed, in all of the above-mentioned devices, a 2-D free-carrier gas under the gate is present (2DEG for GaN and 4H-SiC and 2-DHG for diamond), while the region between the gate and source is almost in ohmic regime (for the applied voltages and considered geometries): an analogous behavior is therefore expected. In contrast, the maximum oscillation frequency could positively benefit from gate–source scaling, as pointed out in [23]. However, this could not be verified on the available diamond devices, since they were not explicitly designed to be RF tested, as noted in Section III.

To evaluate the effect of scaling on the maximum attainable output power densities, a thorough investigation on breakdown voltage was performed as well. It is expected that a shorter L_{GS} corresponds to higher carrier densities under the gate metal and to higher peaks of the horizontal electric field under the drain side of the gate. As the field reaches values high enough to establish avalanche multiplication in the device, the carrier concentration determines how steeply the current will grow up to the eventual burnout of the device.

Obviously, the higher the carrier concentration, the sooner breakdown will occur. This is confirmed by the experimental results reported in Fig. 5, where the drain current of several devices is plotted against the drain–source voltage, V_{GS}, while keeping V_{GS} at 0 V.

The experimental results for devices with $L_{GS} \sim 1$ μm allow estimating a breakdown voltage of about 80 V, although a noticeable spread in the order of ± 10 V is observed. Such a fluctuation can be attributed to nonuniformities of the measured devices, with special reference to the reproducibility of L_{GS} values. For devices with $L_{GS} \sim 2$ μm, no breakdown was observed for voltages up to 100 V, which represents the limit of the power supply available during measurements.

This implies that breakdown voltages $|V_{BK}|$ well beyond 100 V can be obtained by simply setting an appropriate L_{GS}. However, this parameter cannot be increased arbitrarily, in a tradeoff with other figures of merit requiring low L_{GS} values to be optimized.

Fig. 6 shows the I–V characteristics of four device geometries, differing in L_{GS}, but with a common L_{DS} of 6.5 μm.

The dc characteristics confirm the above remarks, showing that the maximum output current density strongly depends on L_{GS}. In particular, higher currents correspond to shorter L_{GS} distances, as already noted in Fig. 2. Moreover, the slope of I_D versus V_{DS} in the ohmic region (before the knee of each trace) is independent on L_{GS} as expected. In addition, other conditions being equal, the knee voltage in the dc characteristics can be lowered by acting on L_{GD}, which must be scaled down. This is demonstrated in Fig. 7, which shows

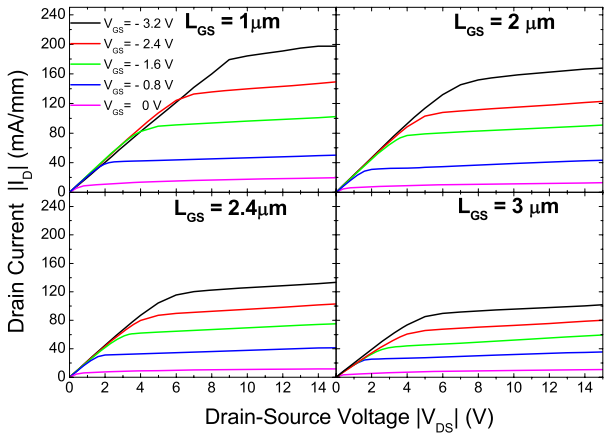

Fig. 6. Drain current density as a function of V_{DS}, with V_{GS} as a parameter, for several L_{GS} values and $L_{DS} = 6.5$ μm.

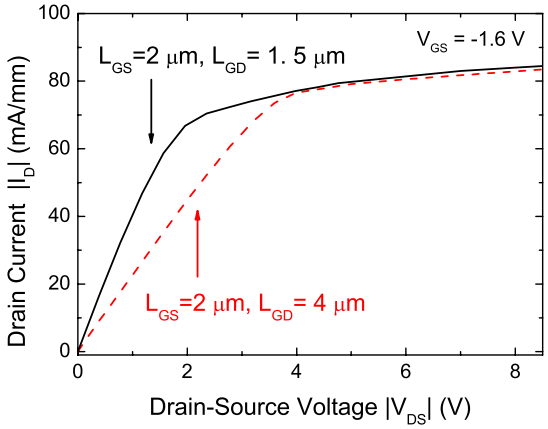

Fig. 7. Drain current density as a function of V_{DS}, for $V_{GS} = -1.6$ V, with constant L_{GS} and two L_{GD} values.

how the slope of the I_D–V_{DS} curve improves significantly by reducing L_{GD} from 4.0 to 1.5 μm, while L_{GS} is held constant (2 μm in this example). This can be explained by recalling that the saturated current of the two devices here considered must be approximately equal (since it depends on L_{GS} only in good approximation), while the saturated current regime will occur earlier in the device with shorter L_{GD} (due to the electric field in the gate–drain area increasing more rapidly).

As a consequence, the drain current of the device with $L_{GD} = 1.5$ μm must reach the saturated value faster than the one with $L_{GD} = 4$ μm as the drain voltage is increased.

The results presented in this section constitute a valuable set of guidelines that, in addition to other well established rules, can help find the optimum tradeoff among often contrasting performance parameters. As an example, these results were used by the authors as a reference to optimize the geometry of a subsequent family of diamond-based MESFETs designed for RF operation. In particular, gate–source and gate–drain distances were minimized by setting $L_{DS} = 1.5$ μm and centering the gate finger, whose length L_G was set to 0.5 μm.

Fig. 8(a) shows the measured dc curves of one such optimized device, whereas Fig. 8(b) shows a detail of the gate profile of the realized transistor. As it can be noted from the

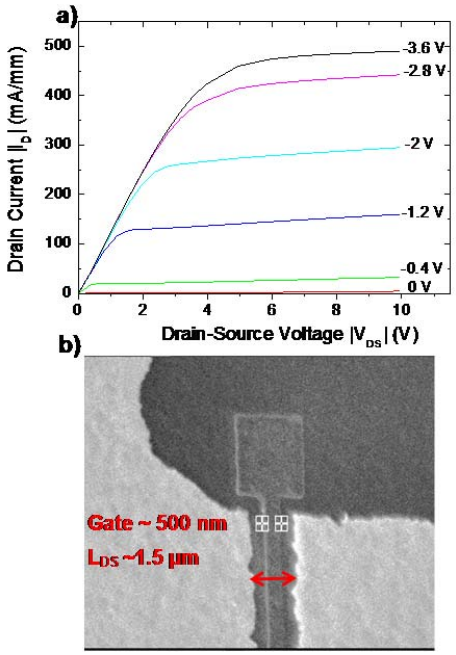

Fig. 8. (a) Drain current density as a function of V_{DS}, with V_{GS} as a parameter, of an RF device with periphery 2×50 μm and $L_G = L_{GS} = L_{GD} = 0.5$ μm. (b) SEM picture of the channel geometry.

I–V graph, saturated drain current densities as high as about 500 mA/mm have been obtained.

V. Conclusion

In this paper, the influence of gate–source and gate–drain distances on the diamond-based MESFET dc characteristics is investigated. The experimental results show that the scaling of the source–gate distance is a key factor for enhancing device performance, with positive consequences on both the output current density and device transconductance. In particular, with the decrease in L_{GS} from 2 to 1 μm, the value of g_m increases from 40 to 85 mS/mm. On the contrary, the device threshold voltage is almost independent of L_{GS}.

In addition, the influence of the different gate position in a fixed drain–source channel has been demonstrated. An increase in the maximum drain current density I_D has been experimentally shown by shortening the gate–source distance.

However, L_{GS} scaling affects the breakdown voltage of the device. For $L_{GS} \sim 1$ μm, the breakdown voltage was measured for different devices in the range 70–90 V.

Finally, keeping a constant gate–source distance, the knee voltage decreases by reducing the total length of the channel (drain–source distance).

The obtained results can be used as a design guideline for the layout of H-terminated diamond MESFETs with optimized performance.

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